Wednesday, June 6

Session 5 - Keynote

Session Chair: Todd Ryan

8:15 am
CMOS/Cu BEOL Technology in Manufacturing: 20 years and Counting, Dan Edelstein, IBM

This keynote speech will recount some key innovations, anecdotes, and milestones associated with the development and implementation of Cu BEOL into CMOS manufacturing 20 years ago, and carry this discussion through its evolution to the present time, and its future prospects.

Last year marked the 20th anniversary of IBM's industry-first CMOS/Cu BEOL technology to reach early production. The subsequent manufacturing volume-ramp in mid-1998 provided the first market for CMOS CPU and other high-performance logic chips with Cu BEOL. The salient features of the original technology definition that was implemented here have largely endured to the present day, though with steady evolutionary improvements. These original features included multilevel Cu dual damascene integration, a TaN/Ta bilayer liner, PVD Cu-seed with electroplated Cu fill, 2-step CMP, a PECVD Si3N4 barrier cap with NH3-based plasma preclean, and SiO2 interlevel dielectric. As well, architectural features enabled by Cu damascene included large-range plane-pair hierarchical wire scaling, from low-C/high-density/short-length fine levels to low-R/long-length global levels, and Al-based transitions to wirebond and C4 terminals. With proper integration techniques with these materials and interfaces, we were able to realize Cu's promise of many orders of magnitude longer electromigration lifetimes than the Al(0.5%Cu) alloy that it replaced. This last aspect has fundamentally kept Moore's Law scaling alive for the BEOL wiring, which would otherwise have broken with Al(Cu) long ago.

Now in its 10th generation of CMOS manufacturing, and 12th generation in the research phase, we are finally starting to see changes beyond evolutionary in the materials and processes, with the end in sight for the Cu finest wires in perhaps 1-2 more generations. However, our current data for recent innovations still suggests this Cu/alternate metal crossover point may be pushed off at least once more beyond some predictions.

Session 6 - Process Integration 2

Session Chairs: Susumu Matsumoto, Hui Jae Yoo

9:05 AM 6-1
Ru liner scaling with ALD TaN barrier process for low resistance 7 nm Cu interconnects and beyond, K. Motoyama, O. van der Straten, J. Maniscalco, H. Huang, YB. Kim*, JK. Choi*, JH. Lee*, C.-K. Hu, P. McLaughlin, T. Standaert, R. Quon, and G. Bonilla, IBM Research, *Samsung Electronics Co. LTD.

Low resistance Cu interconnects with CVD Ru liner have been demonstrated for 7 nm node. Ru liner thickness reduction has been achieved by replacing PVD TaN with a bilayer PVD Ta and ALD TaN stack, while maintaining adequate Cu fill performance. The newly proposed barrier stack (PVD Ta/ALD TaN) with thin Ruliner studied in this paper also enabled a significant Ru CMP performance improvement by mitigating two major Ru CMP issues: Cu recess of narrow lines, and trench height variability between dense and isolated patterns. Furthermore, this novel barrier stack with Ru liner could attain void-free Cu fill even for beyond 7 nm node dimension. Thus, the PVD Ta/ALD TaN/CVD Ru liner is a promising candidate as the liner for Cu interconnects of 7 nm node and beyond.

9:30 AM 6-2

Modified ALD TaN Barrier with Ru Liner and Dynamic Cu Reflow for 36nm Pitch Interconnect Integration, P. Bhosale, J. Maniscalco, N. Lanzillo, T. Nogami, D. Canaperi, K. Motoyama, H. Huang, P. McLaughin, R. Shaviv*, M. Stolfi*, R. Vinnakota*, G. How*, S. Pethe*, b. Sheu*, x. Xie*, L. Chen*, IBM Research, *Applied Materials

Integration of thermal atomic layer deposition (ALD) TaN films modified by physical vapor deposition post-treatment (PPT) and in-situ plasma treatment (IPT) was investigated on 36nm pitch BEOL structures. The PPT and IPT processes produce an interface more suitable for liner (Co/Ru) and physical vapor deposition (PVD) of Cu seed. This results in improvement in Cu gap-fill for both traditional Cu seed/plating process with 15 Å chemical vapor deposition (CVD) Co liner and dynamic PVD Cu reflow (DCR) on 20 Å CVD Ru liner. The PPT also decreased via resistance (R) by sputtering TaN at bottom of the via. IPT processes densify the ALD films and improve EM performance. A promising integration scheme of 20 Å ALD+IPT TaN/20Å Ru/DCR was developed with 20X improvement in electromigration.

9:55 am BREAK

Session 7 - Reliability

Session Chairs: Roey Shaviv, Kazuhoshi Ueno

10:15 AM 7-1

Microstructure Evolution and Implications for Cu Nanointerconnects and Beyond

Szu-Tung Hu[1], Linjun Cao[2], Laura Spinella[3] and **Paul S. Ho**[1], [1]The University of Texas at Austin; [2]GLOBALFOUNDRIES; [3]National Renewable Energy Laboratory

The continued scaling of Cu low k technology is facing serious challenges imposed by basic limits from materials, processing and reliability. This has generated great interests recently to further develop Cu nanointerconnects and alternates, particularly Co and Ru nanointerconnects beyond the 10nm node. The performance and reliability are important considerations for the development of nanointerconnects in addition to challenges from processing complexity and manufacturing cost. In this paper, we investigate the microstructure evolution in Cu, Co and Ru nanointerconnects and the effects on resistivity and electromigration (EM), two key factors contributing to the RC delay and reliability of the nanointerconnects.

The scaling effect on microstructure of Cu interconnects was analyzed down to the 24 nm linewidth for the 14 nm node using a TEM-based high-resolution diffraction technique with capabilities to map in detail the orientation and size distribution of individual grains [1]. The TEM observation was supplemented by a Monte Carlo simulation for grain growth based on local energy minimization, taking into account orientation-dependent grain boundary, strain, and interface energies in order to examine the effect of scaling and material properties on grain growth [2, 3]. The results of this study revealed a consistent picture of microstructure evolution with scaling in Cu nanointerconnects. With the linewidth exceeding 180 nm, a dominant growth of the (111) grains which have the lowest grain boundary energy was observed from the trench bottom, a process controlled by the interface energy. As scaling reduces the linewidth to 120 nm, the growth of the (111) grains began to shift to the trench sidewalls, reflecting the change in the aspect ratio but still interface energy controlled. Twin boundaries were readily observed although only a small fraction being the Σ3 coherent boundaries, which is induced by the strain energy during annealing converting some (111) to (200) grains in order to minimize the elastic anisotropy of Cu. The amount of twin boundaries continued to decrease with scaling and reached to ~1% at 70nm linewidth while small grains emerged near the trench bottom. With further scaling to the 45 nm linewidth (28 nm node), the growth of (111) grains shifted again to along the trench length direction, a trend which continued to the 22 nm linewidth with the appearance of more small grain aggregates, indicating further dominance of the interface energy in comparison to the strain energy with increasing surface to volume ratios.

The result of the microstructure study was used to analyze the scaling effect on the resistivity of Cu nanointerconnects and EM lifetime. We are able to account for the scaling effect on resistivity from the contributions of surface and grain boundary scatterings as reported in a recent study [4]. The scaling effect on EM lifetime was analyzed based on a recent study reporting excellent lifetime and high (1.5-1.6eV) activation energy for the 24 nm Co-capped Cu nanointerconnects [5]. We found that based on the microstructure of the 24 nm Cu nanolines, this will require the Cu grain boundaries to be de-activated, perhaps by "stuffing" with Co atoms as observed in the EM study. Finally, microstructure evolution studies were carried out for Co and Ru by simulation and some limited TEM observations. Results will be reported together with model analyses of the scaling effect on Co and Ru resistivity and electromigration.

10:45 AM 7-2

Electromigration and Thermal Storage study of Barrierless Co vias, O. Varela Pedreira, K.Croes, H. Zahedmanesh, K. Vandersmissen, M. H. van der Veen, V. Vega Gonzalez, D. Dictus*, L. Zhao**, A. Kolics**, Zs.Tőkei, Imec vzw, *Lam Research Belgium, *Lam Research Corp. Fremont, CA

We study the reliability performance in terms of electromigration and thermal storage of barrierless Co vias. While for our reference with Cu filled vias and a TaNCo barrier/liner system we did observe voids in some vias after electromigration, these voids were not observed for the Co vias and thus the studied system is more scalable towards smaller vias. Long thermal storage measurements show more failures in barrierless Co vias. As this problem is linked to a weak Co/dielectric interface and Co/Cu-intermixing, a better adhesion between the Co and the low-k, the use of a non-porous low-k dielectric and the use of a barrier at the via bottom could help to reduce this phenomenon.

11:10 AM 7-3

Pathfinding of Ru-Liner/Cu-Reflow Interconnect Reliability Solution, Z. Wu, F. Chen, G. Shen, Y. Hu, S. Pethe, J. J. Lee, J. Tseng, W. Suen, R. Vinnakota, K. Kashefizadeh, M. Naik, Applied Materials, Inc.

Ruthenium (Ru) and Copper (Cu) interface promotes void-free Cu gap-fill through a Cu reflow approach. However, reliability issues such as Electromigration (EM) and time-dependent dielectric breakdown (TDDB) have delayed industry adoption of Ru liner. Here, we report our findings on two EM improvement approaches and compare them to industry standard Cobalt (Co) liner/selective Co cap based Cu interconnect. Similar to Co liner, addition of a post chemical mechanical planarization (CMP) selective Co cap did improve EM performance with Ru liner. However, EM equivalence to Co liner/Co cap based Cu interconnect requires the development of a new doped Ru liner in combination with the selective Co cap. We will also discuss the impact of the EM improvement approaches on key parameters of interest such as via resistance, TDDB and provide a technology scorecard.

11:35 PM 7-4

Testing The Limits of TaN Barrier Scaling, C. Witt, K.B. Yeap, A.Lesniewska*, D.Wan*, N.Jordan*, I.Ciofi*, C. Wu*, Z. Tokei*, GLOBALFOUNDRIES, *IMEC

The thickness limit of PVD TaN diffusion barrier plus either Co or Ru liner was studied by TDDB testing. A special planar metal-insulator capacitor has been used for this purpose. The TaN range was 0.2 to 3nm, deposited by a low power PVD process. It is found that both Co and Ru liners can add significantly to the barrier integrity. TaN can be thinned to <0.8nm in conjunction with Co. The combination of TaN and Ru showed excellent barrier properties, with TaN as thin as 0.5nm. The impact on line and via resistance is being discussed.

12:00 pm LUNCH

Session 8 - Materials and Unit Process 1 - Dielectrics

Session Chairs: Bryan Hendrix, Tatsuya Usami

1:15 PM 8-1

ALD/Surface functionalization for Conductivity (Invited), Han Bo Ram Lee, Incheon National University

Atomic layer deposition (ALD) is a thin film deposition method employing self-saturated surface reactions. Since ALD has several superior properties for nanoscale device fabrications, such as excellent conformality, large area uniformity, and process compatibility over the conventional thin film deposition methods, it has been widely applied for various high technology applications from semiconductor to display devices. Due to the surface reaction mechanism, ALD can be an effect route to change and modify surface properties with precise controllability in other applications. In this work, we utilized ALD as a tool for surface property modification, in particular, two examples were introduced, improvement conductivity of graphene and organic textiles. Ideally, graphene has high conductivity due to its unique atomic structure, however, it is not achievable in real system because of inevitable formation of defects during synthesis process which deteriorates the conductivity. Pt was selectively formed on the defect sites of chemically-synthesized graphene layer by ALD to improve the low conductivity of graphene, and Pt-decorated graphene was applied to transparent conducting heater system. Fabrication of conductive textiles is important to enable wearable electronics. Inspired from the conventional dyeing technology, we coat textiles with ALD Pt and Ru through organic-inorganic hybridization in atomic level. A capacitive type pressure sensor was fabricated by using the highly conductive ALD-modified textile fibers, and applied to seat sensor for vehicle. The ideas in these two examples could be also applied to other applications which require surface modifications and conductivity improvement without significant change of original properties.

1:45 pm 8-2

Nonaffine Deformations in ULK Dielectric Glasses, K.I. Kilic, R. H. Dauskardt, Stanford University

Our manuscript points out for the first time to the relation between small scale deformation characteristics of ULK dielectric glasses and their mechanical properties. This is a crucial result in the sense that it provides an insight towards which molecular level parameters are controlling thestiffness of ULK organosilicate glasses. Revelation of the connection between deformation characteristics and mechanical properties is a strong step towards designing mechanically more robust and reliable ULK dielectric glasses.

2:10 pm 8-3

Effect of thermal annealing on low-k dielectrics for iBEOL in view of 3D sequential integration, S. Beaurepaire, V. Jousseaume, P. Gonon*, A. Bsiesy*, C. Guérin, N. Rochat, C. Licitra, P-L. Charvet, M. Veillerot, N. Rambal, D. Nouguier**, D. Ney**, X. Federspiel**, C. Fenouillet-Béranger, CEA-Léti, *LTM-UGA, **STMicroelectronics

This work presents an in-depth study of the thermal stability of low-k material in view of intermediate Back-End-Of-Line (iBEOL) for 3D sequential Integration. SiOCH ULK were analyzed after thermal annealing up to 600°C. Moreover, the stability and reliability of this ULK material coupled with W metal in line 1 integration is characterized up to 550°C, 5h. We have demonstrated that low-k material can support a thermal budget of 500°C, 2h with limited outgassing. This result is fully compatible with 3D sequential integration.

2:35 pm
BREAK

Session 9 - Design/Technology Co-optimization

Session Chairs: Mehul Naik, Xiaopeng Xu

2:55 PM 9-1

BEOL Layout Design Considerations To Mitigate CPI Risk (Invited), **Mohamed A. Rabie**, Thiagarajan Raman, Fahad Mirza, Nicholas A. Polomoff, Danish Faruqui, Scott Pozder, Md Khaled Hassan, Tamer Desouky, and Carole Graas, GLOBALFOUNDRIES

We present a summary of some of the main Back End of Line (BEoL) design optimization techniques to mitigate Chip Package Interaction (CPI) risk in flip-chip configuration. Optimization techniques include metal tiles right on top of the metal stack at the corner of the die beyond the bumps, diagonal final aluminum cap metal lines under the corner bumps, octagon shape of the pads under the bumps, 80^{o} PSPI angle opening, as well as wider double rail crackstops.

3:25 PM 9-2

System-level impact of interconnect line-edge roughness, R. Baert, I. Ciofi, Ph. Roussel, L. Mattii*, P. Debacker, Zs. Tokei, IMEC, *Braunschweig University of Technology

This paper provides an analysis of the impact of LER from wire resistance to system-level performance. Our silicon-calibrated resistance model is extended to include the effect of both LER standard deviation and correlation length. The new resistance model is validated against simulations after process emulation. A CPU design is used as benchmark to assess system-level impact by propagating the wire resistance probabilities through the timing analysis to obtain a critical-path timing distribution. Results show that while there is a significant impact of LER on the resistance distribution for short wires, the effect largely averages out on system level.

3:50 PM 9-3

Impact of Line and Via Resistance on Device Performance at the 5nm Gate All Around Node and Beyond, N. Lanzillo, K. Motoyama, T. Hook, L. Clevenger, IBM

This work explores the impacts of line and via resistance on overall device performance (delay, frequency vs. power) across several past and future technology nodes, including 7nm, 5nm and 3nm. This multi-scale approach employs ab initio calculations of via resistance, finite-element calculations of line resistance, and performance modeling taking into account BEOL parasitics.

4:15 PM 9-4

Interconnect-device co-optimization for field-effect transistors with two-dimensional materials, D.Verreck, G.Arutchelvan*, I.Ciofi, M.M.Heyns*, I.P.Radu, imec, *KU Leuven

The interconnect load is often disregarded in the optimization of exploratory device technologies such as field-effect transistors (FETs) with two-dimensional materials (2D). Here, we therefore combine a calibrated device model for bilayer MoS2 FETs with a three-level Cu-TaN/Ru interconnect scheme to show that the highly resistive nature of 2D FETs requires a significant decrease in wire dimensions from the nominal N5 values to achieve optimal delay. We compare a single to a double gate configuration and find the improved drive in the latter results in a lower delay at slightly increased power. In the presence of spacer regions, the extra gate also prevents a dramatic delay increase. Finally, we project that material and contacting improvements allow for a relaxation in wire dimensions.

Session 10

4:40 pm - Poster Session and Reception

10.1

Tungsten Plug Missing Defects Monitoring Method and Its Solution by Optimization of Polymer Cleaning and Micro-environment, Rongwei Fan*, Hunglin Chen, Kai Wang, Yin Long, Qiliang Ni,Shanghai Huali Microelectronics Corporation

This paper describes the tungsten (W) missing defects monitoring method with electron-beam inspection systems, and its solution by optimization of polymer cleaning and micro-environment. W missing defects detection and monitoring method was developed and fixed on bare silicon wafer. Then a series of experiments was carried out, and W missing defects were fixed by the optimization of polymer cleaning and micro-environment of the front side open unit port (FOUP).

10.2

Silicon Trench Etch Uniformity Improvement for Microloading and Macro-to-Macro Loading for sub-14nm Node, Y. Yang, S. Lim, J. Hong, M. Park, Y. Yang, W. Cho, C. Adams, M. Aminpur, and C. Maeng, GLOBALFOUNDRIES

We report a test and demonstration of plasma etching conditions that can be applied in advanced nodes beyond 14nm patterning to relieve trench depth sensitivity to incoming CD variations caused by multipatterning and macro-to-macro loading impacts from pattern density. Our result showed that lower RF duty cycle, higher bias voltage, and higher etchant flow can reduce 50% of the depth variation to incoming CD variations caused by multipatterning in previous steps and 75% of the depth differences between dense and isolated pattern areas for macro-to-macro loading.

10.3

Modulation of Within-wafer and Within-die Topography for Damascene Copper in Advanced Technology, W.-T. Tseng, T.-J. Cheng, S. Ahmed, J. Lee, F. Baumann, GLOBALFOUNDRIES

A novel copper electroplating and CMP process was developed to effectively modulate the within-wafer and within-die nanoscale topography. The feasibility of this new metallization is demonstrated on a 64nm pitch product with an equivalent defect level, lower and tighter distribution in resistance and trench height. It's believed to be extendable to other advanced nodes for a sizable reduction in copper overburden which saves CMP polish cycle time from the plan-of-record time.

10.4

The impact of solute segregation on grain boundaries in dilute Cu alloys, Takanori Tsurumaru, Luke Prestowitz*, Brendan O'Brien* and Kathleen Dunn*, SUMCO Corporation/State University of New York Polytechnic Institute, *State University of New York Polytechnic Institute

Alloying copper with cobalt may offer a means for stabilizing grain boundaries against electromigration void formation in advanced interconnects. Here we present a means for co-depositing dilute copper alloys, using Co and Ag as the solutes of interest. Microstructure and compositional analysis are presented.

10.5
Modeling wafer bending effects on RDL layer reliability in a multiple die package, Tzu Chen Wang, Chih Chieh Yeh, Xiaopeng Xu, Karim El Sayed, Chun-Hung Steven Lin*, Synopsys Inc., *Corning Display Technologies

Wafer bending effects on re-distribution layer (RDL) reliability in a multiple die package is examined using multiscale TCAD sub-modeling techniques. At the global scale, the wafer package with 200 dies and 3 RDL layers is analyzed with smear material representation. At the die scale, three dies from the center, middle, and edge of the package wafer are analyzed to examine the die location effect during wafer bending. At the RDL local scale, wafer bending and layout pattern effects on RDL reliability are examined. Between the scales, TCAD sub-modeling with buffer region technique is employed to extract upper scale solution as boundary constrains for lower scale analyses. The study also considers material effects with temperature dependent material properties and plastic deformation during thermal cycles.

10.6
Silicide based low temperature and low pressure bonding of Ti/Si for microfluidics and hermetic-sealing applications, C.Hemanth Kumar, Asisa Kumar Pnaigrahi*, Satish Bonam, Nirupam Paul, Siva Rama Krishna Vanjari, Shiv Govind Singh, Department of Electrical Engineering,Indian Institute of Technology Hyderabad,*Department of Electronics & Communication Engineering,Koneru Lakshmaiah Education Foundation- Hyderabad.

In this work, we have shown and validated bonding of titanium (Ti) coated glass with (100) silicon wafer at lower thermocompression cycle of 377 ˚C temperature and a nominal contact pressure of 0.15 MPa. Excellent bond strength > 100MPa and void free interface have been observed using scanning acoustic tomography (SAT), which clearly suggest that optimized temperature-pressure together can provide a superior quality bonding. Furthermore, post-bond dicing was performed in order to validate further the bonding strength which was confirmed by successfully dicing the Glass-Silicon pair without any damage to the bonding interface. This noble, low cost and low temperature simple bonding approach must be useful in hermetic sealing of microfluidic channels for on-chip compatible applications

10.7
A Highly Reliable 1x5um Via-last TSV Module, Stefaan Van Huylenbroeck, Yunlong Li, Joeri De Vos, Geraldine Jamieson, Nina Tutunjyan, Andy Miller, Gerald Beyer, Eric Beyne, imec

A 1x5um via-last TSV module is presented, coping with the reliability challenges imposed when exposing the metal landing pad during the liner opening etch at the TSV bottom. Two approaches are presented. A dedicated soft-landing liner oxide dry etch step is developed, eliminating the re-sputtering of copper on the TSV sidewalls. An embedded barrier is integrated, blocking the diffusion of any eventually re-sputtered copper of the landing pad. The obtained via-last TSV reliability is high for both approaches.

10.8
Strategy of Insertion of Merge Features in a Sea of Wires SADP Integration, J. H.-C. Chen, T. A. Spooner, L. A. Clevenger, M. O'Toole*, A. Ogino*, L. Lanzerotti*, S. Reidy*, C. Child*, IBM, *GLOBALFOUNDRIES

In BEOL, not only the minimum features, but wide lines are also important for power distribution. However, in the conventional SADP integration, insertion of wide features in the sea-of-wires area cannot be achieved easily. In this paper, five process schemes for insertion of complicate shapes were presented in this paper. These processes are designated as add on modules to boost the performance of the conventional SADP integration.

10.9

A Study on SADP Process Refresh for Patterning Correction, J. H.-C. Chen, I. C. Estrada, C. B. Peethala, Y. Mignot, H. Shobha, T. E. Standaert, IBM

In SADP integration, an accurate CD and profile control of mandrel patterning is important and an incorrect mandrel CD or profile could cause a huge loss. In this paper, a novel methodology suitable for high volume manufacturing is presented to remove the incorrect patterning stack and to refresh the SADP patterning from the beginning. As a result, the misprocessed wafer could continue the process without loss. Similar approaches could also be applied to FIN module.

10.10

Impact of Sn content in Ge1-xSnx layers on Ni stanogermanides solid-state reaction and properties, A. Quintero* **, P. Gergaud*, N. Chevalier*, J. Aubin*, J. M. Hartmann*, V. Loup*, V. Reboud*, E. Cassan** and Ph. Rodriguez*, * CEA LETI, ** CNRS, C2N

A comprehensive analysis focused on the impact of Sn content in GeSn layers, on Ni-based contacts, is presented. In-situ XRD, AFM and Rsh measurements were performed in order to follow phase growth, surface morphological evolution and electrical properties as the annealing temperature changed. Potential impact of those evolutions on devices integration is also discussed.

10.11

Effective Methods Controlling Cu Overburdens for Cu RDL Process, K. Park, J. Lee, B Yoo, Hanyang University

Microcontact printing (μCP) and electrochemical polishing (ECP) were proceeded for the Cu overburden thickness reduction and Cu planarization during the redistribution layer process. The suppressing property of μCP and the polishing effect of ECP were confirmed by electrochemical analysis. Suppressing effect of top surface of trench was confirmed after the μCP and Cu filling, and the removal of Cu overburdens was also confirmed after the Cu filling and the ECP.

10.12

Physical and Electrical Properties of New Zr Precursors with High Thermal Stability for High-k, H. D. Lim, S. Y. Jeon, W. M. Chae, J. J. Park, S. J. Yim, S. I. Lee, M. W. Kim, DNF Corporation

New Zr precursors have been developed using a tri-amine structure with enhanced thermal stability. The ALD window of the tri-amine structure is 220 to 320 degrees Celsius. In the capacitor structure with aspect ratio of 60 to 1, the step coverage was 99 percent. The dielectric constants of the ZrO2 thin films using tri-amine structure were improved by up to 13 percent and the leakage currents were similar to those of the cyclopentadienyl structure.

10.13

Oxidation Structure Change of Copper Surface Depending on Accelerated Humidity, P. Gomasang, S. Ogiue, K. Ueno, S. Yokogawa*, Shibaura Institute of Technology, *The University of Electro-Communication

For long-term reliability of Cu film in an environment, humidity dependence of the sheet resistance increase has been studied. We observed that resistance increase at 85% RH was almost the same to that of 75% RH in spite of higher oxidation. The nonlinear phenomena can be explained by the difference in the Cu oxide structure. The results suggest that lower humidity acceleration will be more appropriate in the THS test for passivated Cu to estimate the moisture resistance life because the real usage is typically in lower humidity.

10.14
Non-Reagent Express Metrology for Modern Damascene Copper Plating Baths, Michael Pavlov, Danni Lin, ECI Technology

The capability of analyzing all components in modern copper electroplating baths using non-reagent methods is demonstrated. The concentration of copper in new plating baths is significantly lower than in traditional baths. This article presents the results of our most recent study of the behavior of organic additives at low copper concentrations. The analytical results of our new methods for all bath components are presented.

10.15
Stress induced densification of thin porous low-k films during nanoindentation, O. O. Okudur*, M. Redzheb**, K. Vanstreels**, H. Zahednamesh**, M. Gonzalez**, I. De Wolf*, *KU Leuven and imec, **imec

Simultaneous impact of the substrate and pore densification hinders their differentiation during nanoindentation of porous thin low-k films, causing significant loss of valuable information in terms of nonlinear mechanical behavior. In this paper, we propose a method to overcome this issue by utilizing three nanoindenter probes that generate substantially different stress levels and elastic field distributions. The experimental results are benchmarked with FE simulations using Gurson model for porous media. The proposed multiple-probe approach could facilitate non-linear property characterization of fabricated low-k materials.

10.16
Integration of Metallization Processes in Robust Interconnects Formation for 14 nm Nodes and beyond, Nicolai Petrov, Shao Beng Law, Jonathan Rullan, Seungman Choi, San Leong Liew, Han Wah Ng, Shinichiro Kakita, GLOBALFOUNDRIES

In this communication the results of metallization processes integration to create robust Cu interconnects for advanced 14 nm and beyond nodes are presented. Conventional Dual Damascene BEOL process flow to form 64 nm pitch on-chip Cu interconnects in low-k dielectric substrate was utilized. TaN/Ta/Cu seed were formed by PVD, Cu lines were fabricated by Cu ECP followed by CMP.

10.17
Electrolytic Cobalt Fill of Sub-5 nm Node Interconnect Features, F. Wafula, J. Wu, S. Branagan, H. Suzuki, A. Gracias, J. van Eisden, Atotech USA LLC.

Electrolytic cobalt fill of sub-5 nm node features and a proposed model for the fill mechanism supported by cyclic voltammetry is presented. The transformation of the organic plating additive from an active to a de-activated state at the bottom of the feature is suggested as the mechanism of cobalt bottom-up fill. Plating results in features with 2- and – 4 nm pre-plate openings show void-free fill.

10.18
An Innovative System Integration Interconnection Technology Beyond BEOL, Dyi-Chung Hu, SiPlus Co.

The goal of this study is to verify an innovative system integration technology that integrates the connections beyond the I/Os of the chips. As the signals come out from the IC chip, it passes through UBM, bumps and solders in order to connect to the outside world. But the line density of the substrate underneath the die can’t shrink as fast as the Moore’s law. Hence the packaging industry developed the interposer (2.5D) on top of the substrate to solve the fine line requirement of substrate. The advanced chip packaging structure includes components of interposer, substrate and PCB. Each connection component needs a core to support during manufacturing process. The final packaging structure uses solders to connect between

interposer, substrate and PCB. The solders are left in the final packaging structure. In this paper, a new structure that do not need the cores and most of solders in the final packaging structure is proposed and tested. This new system integration packaging structure is a solder-minimum, TSV-less and core-less structure. A test chip with 10,000 bumps and 50µm pitch has been designed and manufactured to test this new structure. This new substrate structure composed of two portions; thin film fine line and laminated dielectric. The dimensional changes of the new test substrate were under control to be less than 4µm in 10mm range. Further bonding of the test chips to the new substrate was verified using a commercial TCB bonder.

10.19
Gas Phase Pore Stuffing (GPPS), M. Fujikawa, T. Yamaguchi, S. Nozawa, R. Niino, R. Chanson*, K. Babaei Gavan*, F. Lazzarino*, J-F. de Marneffe*, Tokyo Electoron Technology Solutions Limited, *Imec v.z.w.

Porous low-k dielectrics play an important role in lowering the circuit capacitance in nano-interconnects. However, these materials are damaged during plasma etching process and subsequent steps, leading to a degradation of their dielectric properties. We suggest a new method to solve the issue, so-called Gas Phase Pore Stuffing (GPPS). GPPS can fill the pores with sacrificail polymers by a single-step CVD process, and remove polymer by only Annealing.

10.20
Cu Barrier Properties of Cluster-Preforming-Deposited Amorphous WSin Films Depending on Composition n, N. Okada, N. Uchida, S. Ogawa, T. Kanayama, AIST

The thin amorphous WSin film with n =12 exhibited excellent diffusion barrier properties for Cu: an estimated TDDB lifetime > 10 years at 100 °C under 5 MV/cm stress for Cu MOS capacitors and a high barrier stability against annealing up to 600 °C for Cu on Si diodes. In addition, in the WSin (n =5−12) film in contact with Cu, the Si atoms do not diffuse into the Cu layer in spite of the Si-rich composition even at 300 °C. When n is 12, the WSin film has the most excellent thermal stability. From the ab-initio simulations, these properties are attributed to the fact that in the film, all the Si atoms are strongly bonded to the negatively charged W atoms. These results indicate that the WSi12 film is a promising barrier film against Cu.

10.21
Charge-Trap-Free Polymer-Liner Through-Silicon Vias for Reliability Improvement of 3D ICs, H. Kino, S. Lee, Y. Sugawara, T. Fukushima, T. Tanaka, Tohoku University

In this study, MIS capacitors with blind TSV structures using PI, BCB or PBO liners were fabricated and evaluated. In the case of BCB and PBO liners, remarkable hysteresis suppressions of the C-V curves was observed as compared to that of the PI liner. These results indicate that polar character is one of the most important characters for suppression of the capacitance modulation around TSVs and the detrapped-charge-induced signal noise.

10.22
Spray Plasma Processing of Barrier Films Deposited in Air for Improved Stability of Flexible Electronic Devices, Nicholas Rolston[1], Adam D. Printz[1], Florian Hilt[1], Michael Q. Hovish[1], Karsten Brüning[2], Christopher J. Tassone[2], Reinhold H. Dauskardt[1], [1]Stanford University, [2]SSRL, SLAC National Accelerator Laboratory

We report on submicron organosilicate barrier films produced rapidly in ambient by a scalable spray plasma process for improved solar cell stability. The plasma is at a sufficiently low temperature to be compatible with flexible electronic devices. The morphology and density of the barrier are shown to improve with the

addition of a fluorine-based precursor. Thin-film perovskite solar cells with submicron coatings exhibited significant improvements in stability when exposed to light, heat, and moisture.

10.23
Advanced metallization processes integration as manufacturing worthy solutions for >10:1 aspect ratio mid-process TSV, Thierry Mourier, Mathilde Gottardi, Céline Ribière, Gilles Romero*, Stéphane Minoret, Pierre-Emile Philip*, CEA Leti, *STMicroelectronics

This paper presents the evaluation of alternative metallization solutions able to overcome the actual limitations of TSV form factor and enable >10:1 aspect ratio mid-process TSV. Process choices and development are described and electrical results of the integration of these materials and processes are presented showing excellent yield, performances and distribution

6:30 pm
End of Sessions