Tuesday, June 5

Session 1 – Keynote Session

8:15 am
Welcome, Introduction and Awards, Noel Russell, TEL, General Chairman

8:25 am
Keynote Presentation
The Viability of Quantum Computing from an Interconnects Perspective, James S. Clarke, Intel Corporation

Quantum computing is an emerging compute technology that holds the promise of exponential speedup compared to classical computing for certain applications. Relatively small numbers of logical quantum bits, or qubits, could outperform the largest of supercomputers. For many universities, companies, and governments, this is akin to a modern space race or moon shot. Applications in the areas of chemistry, medicine, machine learning, and cryptography may be enabled with quantum computers where a classical computer could not accomplish the task on any realistic timescale.

Two of the most promising qubit technologies are superconducting qubits and spin qubits in silicon. These technologies bare similarities to the device and interconnect technologies used in advanced CMOS processing today. Examples are shown below. Intel's Tangle Lake 49-qubit superconducting chip is shown on the left while our first 3-qubit spin system is shown on the right. At present, the quantum community is exploring systems comprised of a few 10's of qubits with a long term goal of several million on a single chip. What is the bottleneck to moving beyond few-qubit devices? In a word... Interconnects! Today's qubits have personalities. They are all different. Individual control of each qubit is required, which puts pressure on interconnect topologies and control electronics.

In this talk, we'll introduce the key concepts of quantum computing. Then we'll show the building blocks of the quantum computer including the materials and devices required to operate qubits at temperatures near absolute zero. Finally, we'll talk about the key challenges to go from the few qubit regime to a commercial scale system.

9:15 am
BREAK

Session 2 - Process Integration 1

Session Chairs: Dan Edelstein, Andrew Yeoh

9:35 am 2-1
The Future of Interconnects: Challenges and Enabling Technologies (Invited), Kevin Lin, Manish Chandhok, Miriam Reshotko, Intel Corporation

Enabling resistance and capacitance scaling are key to delivering interconnect performance for future technology nodes [1]. Copper interconnects become less advantageous at smaller dimensions due to the large mean free path of Copper and the need for a diffusion barrier. In addition, electromigration (EM) limits the current density of copper interconnects at small dimensions [2]. Novel barriers for copper may be used to increase the copper volume fraction of an interconnect line, and alternate metals with shorter mean-free-paths (MFP) may offer barrier-free solutions for future technology nodes [3]. To improve capacitance, carbon-doped silicon dioxides (CDO) has been implemented in modern technologies [1]. However, it has been difficult to integrate porous low-K inter-layer dielectrics (ILD) into interconnect systems [1]. This talk

presents opportunities with using pore stuffing to improve patterning to enable low-K integration [4, 5] and the simulated capacitance and performance benefits using pore stuffing technologies.

As interconnect line patterns formed from gratings, pitch-division solutions exist to make interconnect lines that are smaller than the minimum resolvable pitch from lithographic patterning; however, it has become increasingly difficult to print cuts and vias [6, 7]. Existing approaches require multiple passes of cuts and vias, which not only increases the cost, but makes alignment more challenging [6, 7]. In addition, edge placement error (EPE) from various sources such as registration errors, line edge roughness, and critical dimension (CD) variation becomes increasingly important at smaller dimensions [6, 7, 8]. One solution to mitigate via shorting to the wrong line by using hard masks of different materials with high etch selectivity [9]. This talk details the benefits of via shorting improvement through different hard masks, given edge placement error assumptions. Furthermore, using selective deposition may enable self-alignment techniques to reduce total EPE [10].

The overall BEOL interconnect solution is becoming increasingly integrated. Metallization, dielectric, and patterning are challenges have important interdependencies so the interconnect solution needs to be co-optimized. These solutions will be enabled with the advent of new materials and innovative patterning techniques.

10:05 AM 2-2

High-Aspect-Ratio Ruthenium Lines for Buried Power Rail, Anshul Gupta, Shreya Kundu, Lieve Teugels, Jürgen Bömmels, Christoph Adelmann, Nancy Heylen, Geraldine Jamieson, Olalla Varela Pedreira, Ivan Ciofi, Bharani Chava, Christopher J. Wilson, Zsolt Tőkei, Imec

High-aspect-ratio (HAR) Ru power rails, buried in front-end-of-line (FEOL) oxide, can potentially replace conventional middle-end-of-line (MOL) Cu power rails. The HAR feature can boost performance by reducing resistance and voltage drop along the power line. The buried nature, helps to minimize standard cell height by freeing up routing resources at MOL, enabling overall area scaling. This paper demonstrates, Ru lines of aspect ratio up to 7, at a CD of 18 nm. Line resistance at these dimensions, measures at 60 Ω/μm, with the minimum electrical resistivity of 8.8 μΩcm, as extracted from the temperature-controlled-resistance (TCR) measurements. HAR Ru lines are also found to withstand very high FEOL thermal budgets, such as 1000 °C activation anneal for 1.5 s. The combination of all these factors, make HAR Ru buried power rail, a promising scaling booster for next generation technology nodes.

10:30 AM 2-3

Electroless Cobalt Via Pre-Fill Process for Advanced BEOL Metallization and Via Resistance Variation Reduction, J. Gu, D. Zhao, M. Kamon, D. M. Fried, G. Harm*, T. Mountsier*, Coventor, Inc, a Lam Research Company, *Lam Research

While processes have been developed to reduce nominal via resistance due to resistive Ta/TaN barrier layers, little effort has been made to show improvements to counteract the shrinking process window for via resistance with technology dimension. An electroless Co via-prefill process can improve nominal resistance, and in this paper, we quantitatively demonstrate improvement in process variability. Through process modeling with virtual fabrication, we also scale this prediction to 7 nm where the variability of the typical Ta/TaN approach is 50% higher with Co via-prefill.

10:55 AM 2-4
Subtractive Etch of Ruthenium for Sub-5nm Interconnect, D. Wan, S. Paolillo, N. Rassoul, B. K. Kotowska, V. Blanco, C. Adelmann, F. Lazzarino, M. Ercken, G. Murdoch, J. Bömmels, C. J. Wilson, and Zs. Tőkei, imec

Ruthenium has been considered to replace copper in advanced nodes. We fabricated Ru structures using EUV and subtractive etch. Lines with CD<10.5 nm were formed and tested. Using TCR method, resistivities and areas were obtained. Ru lines with AR 3.8 were fabricated and have resistance below 500Ω/μm at 12 nm CD. Ru is expected to outperform damascene Cu at this scale, supporting insertion of subtractive etch Ru for advanced technology nodes.

11:20 AM 2-5
Impact of liner metals on copper resistivity at beyond 7nm dimensions, H. Huang, N. Lanzillo, T. E, Standaert, K. Motoyama, C. Yang, H. Shobha, J. Maniscalco, T. Nogami, J. Li, T. Spooner, G. Bonilla, IBM

The impacts of ruthenium and cobalt liners on copper resistivity have been investigated at beyond 7nm dimensions. Liner metal conduction was carefully evaluated in a Cu resistivity derivation using the temperature coefficient of resistivity (TCR) approach. Cu resistivity with Ru liner is higher than with a Co liner by 10-15%, which is verified by RC plot. The resistivity difference is attributed to interface scattering and possibly grain boundary scattering. Interface ab initio calculations show 3-7% increase of Cu resistivity from Coliner to Ru liner.

11:45 pm
LUNCH

Session 3 - Novel Interconnect Materials and Systems

Session Chairs: Fabrice Nemouchi, Mansour Moinpour

1:00 PM 3-1
Challenges and Progress on Carbon Nanotube Integration for BEOL Interconnects (Invited),
B. Uhlig[1], A. Dhavamani[1], N. Nagy[1], K. Lilienthal[1], R. Liske[1], R. Ramos[2], J. Dijon[2], H. Okuno[3], D. Kalita[3], J. Lee[4], V. Georgiev[4], A. Asenov[4], S. Amoroso[5], L. Wang[5], F. Koenemann[6], B. Gotsmann[6], G. Goncalves[7], B. Chen[7], J. Liang[8] , R. R. Pandey[8], R. Chen[8], A. Todri-Sanial[8], [1]Fraunhofer IPMS, Dresden, Germany; [2]CEA-LITEN/University Grenoble Alpes, France; [3]CEA-INAC/University Grenoble Alpes, France; [4]School of Engineering, University of Glasgow, UK; [5]Synopsys Inc., Glasgow, UK; [6]IBM Research Zurich, Switzerland; [7]Aixtron Ltd., UK; [8]CNRS/LIRMM-University of Montpellier, France

Here, we review and present current challenges and progress on Carbon Nanotube Integration for BEOL Interconnects as well as our recent results. Amongst all the research on carbon nanotube interconnects, those discussed here cover 1) improvement of the variability of SWCNTs for local interconnects 2) process & growth of carbon nanotube interconnects compatible with BEOL integration and formation of CNT-copper-composites, 3) modeling and simulation from atomistic to circuit-level benchmarking and performance prediction, and 4) characterization and electrical measurements. The aim is to evaluate the use of CNT-based materials for future metallization, both in regards to manufacturability, i.e. CMOS compatibility and wafer-scale integration as well as realistic performance expectations, i.e. variability and defectivity.

1:30 PM 3-2
CMOS-Compatible Contacts for Si Photonics From Solid-State Reaction to Laser Integration, E. Ghegin* **, S. Zhiou**, S. Bensalem**, L. Toselli**, M. Pasquali**, S. Favier* **, C. Jany **, B. Szelag**, P. Gergaud**, F. Nemouchi**, Ph. Rodriguez**, * STMicroelectronics, ** CEA LETI

From surface preparation and solid-state reaction to laser integration, a short overview of the CMOS compatible contacts developed in our group on n-InP and p-InGaAs for Si photonic applications is proposed.

1:55 PM 3-3
Single Crystal Al Interconnects Formed on p-GaN and Their Application to GaN FET, Takeshi Harada, Koji Utaka, Yusuke Kanda, Katsuhiko Onishi,Keiichi Matsunaga*, Masahiro Hikita*, Yasuhiro Uemoto*, Panasonic Semiconductor Solutions, *Panasonic

A new technology for manufacturing GaN FET is proposed. A Ti/Al/Ti stackcontacting to p-GaN is used as a gate metal. Surprisingly, Al forms a single crystal. It is due to an epitaxial growth of Al on p-GaN. Sheet resistance of the Ti/Al/Ti stack is decreased by the single crystal formation. Electromigration lifetime is drastically improved with the fraction of the single crystal. In addition, the Ti/Al/Ti stack shows very low contact resistance to p-GaN.

2:20 PM 3-4
Graphene Interconnects – High Performance Twisted 20 nm Graphene Ribbons, X. Wu, A. Contino, B. Soree, M. Heyns, I. Asselberghs*, C. Huyghebaert*, Z. Tokei*, KU Leuven, *IMEC

We investigate the effect of interlayer coupling on the electrical performance of few layer graphene (FLG) interconnects. On SiO2, AB-stacked graphene layers show low carrier mobility due to strong interlayer coupling and formation of parabolic bands. A dramatic increase in carrier mobility and conductivity is observed when the graphene layers are twisted. At sufficiently large angles, single layer graphene (SLG) like behavior is observed in the FLG. Furthermore, the electrical resistance of scaled ribbons down to 20nm width and possible failure mechanisms in graphene wires is investigated. Record values up to 2000cm2/Vs are reported for scaled FLG ribbons below 100nm.

2:45 pm
BREAK

Session 4 - Contacts and Local Interconnects

Session Chairs: Paul Besser, John Zhu

3:05 PM 4-1
Contact Metallization for Advanced CMOS Technology Nodes (Invited), **V. Kamineni**, A. Carr*, C. Niu, P. Adusumilli*, T. Abrams, R. Xie, S. Fan*, J. Kelly*, H. Amanapu*, S. Tsai, K. Ryan, Y. Liang, X. Lin, S. Choi*, H. Dixit, A. Konar, N. Lanzillo*, H. Wu*, J. Cho, D. Guo*, K. Choi*, M. V. Raymond, GLOBALFOUNDRIES Inc.;*IBM

Continuous CMOS scaling is being driven by innovation of novel device architectures to improve device performances at lower power consumption [1]. However, middle-of-the-line (MOL) continues to be a key performance and yield detractor for scaling. To alleviate these challenges, disruptive MOL architectures and materials are being proposed. At the ≤ 10NM node, significant differences are already seen in the MOL architecture and materials used by leading semiconductor companies [2-4]. This is expected to continue to smaller CMOS nodes where contacts represent significant contribution to external resistance (Rext). Figure 1 illustrates the impact of scaling on source/drain (S/D) contact vertical resistance, which can be quantified as the sum of silicide contact resistance (RC) and trench metallization resistance (RTS) [5]. It can be

observed that at ≥ 20 nm trench bottom critical dimension (BCD), silicide contact resistance is the predominant contributor to the total vertical resistance. At these dimensions, it is critical to lower the specific contact resistivity (ρC) to reduce the vertical resistance. At narrow (< 20 nm) dimensions, it is observed that trench metallization resistance (for ρC = 0) contribution to the total vertical resistance starts to increase. In addition, below ~11nm of BCD we see an inflection in resistance because of the change in transport from high resistive nucleation layers to liner/barrier materials. It should be noted that this figure was generated using resistance calculations for a simple trench dimension not specific to any technology and typical MOL materials.

3:35 PM 4-2
Extreme Contact Scaling with Advanced Metallization of Cobalt, Raymond Hung, Jin Hee Park, Tae Hong Ha, Mark Lee, Wenting Hou, Jianxin Lei, Jonathan R. Bakke, Shashank Sharma, Karthik Raman Sharma1, Amir Wachs*, Nam Sung Kim, Ellie Yeh, Applied Materials Inc., Sunnyvale, CA, USA, *Applied Materials Israel, Rehovot, I

Extending tungsten contact for the most advanced nodes (≤ 7 nm) is challenging due to the growing impact of contact resistance on the overall resistance of a device and to the increasing difficulty of gapfill in features with < 20 nm critical dimensions. The paper presents a gapfill material using metal-organic chemical vapor deposition (MO-CVD) cobalt for contact plug.Highlights of new gapfill material include proven seamless, voidless gapfill and contact resistance reduction. CVD Cobalt anneal parameters are discussed that can be optimized in combination with the deposition process to achieve desired gapfill. A proprietary electron-beam imaging technology was used to qualify the cobalt fill for void-free performance. Various process flows are discussed that lead to the best-known fill and resistance reduction values.

4:00 PM 4-3
Replacement Metal Contact Using Sacrificial ILD0 for Wrap Around Contact in Scaled FinFET Technology, S-A. Chew, S. Demuynck, L. Zhang, A. Pacco, K. Devriendt, L. Teugels, T. Hopf, J. Versluijs, C. Vrancken, A. Dangol, E. Altamirano Sanchez, D. Mocuta and N. Horiguchi , Imec, Leuven, Belgium

In this work, we propose replacement metal contact (RMC) flow by using sacrificial ILD0 that is suitable for wrap around contact (WAC). RMC minimize erosion of gate plug, spacer and Source/Drain area at scaled contact formation. The concept of the flow has been demonstrated in short loop flow with ~50% contact resistance improvement for both NMOS, Si:P and PMOS, SiGe:B.

4:25 PM 4-4
Validity and Application of the TCR Method to MOL Contacts, E. Milosevic, V. Kamineni*, X. Zhang**, H. Dixit*, H. Huang***, R. Southwick***, C. Janicki***, N. Lanzillo***, D. Gall, M. V. Raymond* Rensselaer Polytechnic Institute, *GLOBALFOUNDRIES Inc., **Cisco Systems Inc., ***IBM Research

As structure size decreases, electron scattering and liner conduction effects may lead to inaccuracy in the TCR method. To investigate these potential issues for tungsten systems, resistivity, grain size, and temperature derivatives of sheet resistance are measured as a function of thickness for CVD deposited films. Liner conduction was found to impact the apparent temperature dependence of sheet resistance for thin W films. W films exhibit a dρ/dT value 39% higher than reported in literature for bulk. The effect of electron scattering at surfaces and grain boundaries on the temperature derivative of sheet resistance is predicted from common classical scattering models and it is concluded that these mechanisms do not play a significant role. It was also found that TCR accuracy is improved in W contact structures by using the derivative of resistivity determined from the W blanket film analysis. In addition, we also calculated TCR values from first principles which are in good agreement to our experimental results.

4:50 pm Sessions end