Thursday, June 7

Session 11 - Process Integration 3

Session Chairs: Toshiaki Hasegawa, Terry Spooner

8:15 AM 11-1

Interconnect Stack using Self-Aligned Quad and Double Patterning for 10nm High Volume Manufacturing (Invited), **A. Yeoh**, A. Madhavan, N. Kybert, S. Anand, J. Shin, M. Asoro, S. Samarajeewa, J. Steigerwald, C. Ganpule, M. Buehler, A. Tripathi, V. Souw, M. Haran, S. Nigam, V. Chikarmane, P. Yashar, T. Mulé, Y-H. Wu, K-S. Lee, M. Aykol, K. Marla, P. Sinha, S. Kirby, H. Hiramatsu, W. Han, M. Mori, M. Sharma, H. Jeedigunta, M. Sprinkle, C. Pelto, M. Tanniru, G. Leatherman†, K. Fischer, I. Post, C. Auth, Intel Corporation

This paper describes Intel's 10nm high performance logic technology interconnect stack featuring 13 metal layers comprising two self-aligned quad patterned and four self-aligned double patterned layers. Quad patterned interconnect layers are introduced to continue Moore's Law, i.e. sub-40nm interconnect pitches to enable 10nm node cells that include 34nm fin pitch and Contact-over-active-gate (COAG) layout. Cobalt metallization is introduced in the pitch quartered interconnect layers in order to meet electromigration and gapfill-resistance requirements.

8:45 AM 11-2

Process Challenges in Fully Aligned Via Integration for sub 32 nm Pitch BEOL (Invited), **Benjamin D. Briggs**, C. B. Peethala, D. L. Rath, J. Lee, S. Nguyen, N. V. LiCausi*, P. S. McLaughlin, H. You*, D. Sil, N. A. Lanzillo, H. Huang, R. Patlolla, T. Haigh Jr, Y. Xu, C. Park*, P. Kerber, H. K. Shobha, Y. Kim**, J. Demarest, J. Li, G. Lian, M. Ali, C. t Le, E. T. Ryan*, L. A. Clevenger, D. F. Canaperi, T. E. Standaert, G. Bonilla, and E. Huang, IBM; *GLOBALFOUNDRIES Inc.; **Samsung Electronics

As BEOL pitch continues to aggressively scale, contributions from pattern dimension and edge placement constrict the available geometry of interconnects. In particular, the critical minimum insulator spacing which defines a technologies max operating voltage is now limited by Vx to Mx spacing. This spacing has historically been a challenge since the introduction of self-aligned vias due to the loss of CD and chamfer control in the non-self-aligned direction. As pitch continued to shrink from self-aligned via introduction around the 22 nm node, the fraction of via CD control and edge placement compared to the dielectric spacing between interconnects has continued to grow. Alone this trend could be combated by increasing the dielectric spacing, however, the exponential increase in Cu resistivity (under scaling) has forced BEOL technologies into strong line/space asymmetry to keep line resistance under control. At pitches below 32 nm these factors reach a tipping point, either design to exponentially increasing line resistance or lower the technology Vmax. Both approaches cause performance degradation to achieve pitch scaling

9:15 AM 11-3

PVD-Treated ALD TaN for Cu Interconnect Extension to 5nm Node and Beyond, Z. Wu, R. Li, X. Xie, W. Suen, J. Tseng, N. Bekiaris, R. Vinnakota, K. Kashefizadeh, M. Naik, Applied Materials, Inc.

We report a novel approach to enable thin (≤15Å) ALD-based TaN barriers. The use of a post-ALD treatment in a PVD chamber resulted in ALD films with resistivity, density and Ta/N ratio similar to industry-standard PVD TaN. This approach enables conformal Cu barrier without reliability degradation compared to PVD TaN. This new approach overcomes the shadowing effect of the traditional PVD approach, improves the metal-fill process window, and promotes lower via resistance through barrier thickness reduction, proving it to be a viable Cu-barrier candidate for 5nm node and beyond.

9:40 AM 11-4
Interconnect Challenges and Opportunities in the Memory Space (Invited),
John Smythe, Marko Milojevic, Greg Herdt, Sumeet Pandey, Richard Hill, Micron Technology, Inc.

Interconnect requirements of logic and memory share the same categories of mechanical, metallurgical and electrical principles. The details of thermal budget, on-pitch features and aspect ratio have motivated an increase in the number of different approaches. Specific cases will be reviewed that span chemistry, materials, methods and related topics to support the nature of unique challenges within the scope of memory technology scaling.

10:10 am
BREAK

Session 12 - Materials and Unit Process 2 - Metals

Session Chairs: Vimal Manineni, Zsolt Tokei

10:30 AM 12-1
Alternative Metals: from ab initio Screening to Calibrated Narrow Line Models (Invited),
Christoph Adelmann, Kiroubanand Sankaran, Shibesh Dutta*, Anshul Gupta, Shreya Kundu, Geraldine Jamieson, Kristof Moors**, Nicolò Pinna, Ivan Ciofi, Sven Van Elshocht, Jürgen Bömmels, Guillaume Boccardi, Christopher J. Wilson, Geoffrey Pourtois,*** and Zsolt Tőkei, Imec; *KU Leuven, **University of Luxembourg, ***University of Antwerp

We discuss the selection and assessment of alternative metals by a combination of ab initio computation of electronic properties, experimental resistivity assessments, and calibrated line resistance models. Pt-group metals as well as Nb are identified as the most promising elements, with Ru showing the best combination of material properties and process maturity. An experimental assessment of the resistivity of Ru, Ir, and Co lines down to ~30 nm2 is then used to devise compact models for line and via resistance that can be compared to Cu predictions. The main advantage of alternative metals originates from the possibility for barrierless metallization.

11:00 AM 12-2
Metals for low-resistivity interconnects, Daniel Gall

A combination of experiments and first-principles simulations are used to search for metals that have a high conductivity at reduced dimensions and are therefore promising candidates for narrow interconnect lines. Epitaxial layers of Cu, W, Ta, Mo, Ru, Co, Ag, Nb and Ni are grown on ceramic single crystal substrates and their resistivity measured in-situ as a function of thickness. The measured values are directly compared to predictions using first-principles calculations of the most conductive elements.

11:25 AM 12-3
Metallic ceramics for low resitivity interconnects: an ab initio insight, K. Sankaran, K. Moors*, S. Dutta, C. Adelmann, Z. Tőkei, G. Pourtois**, IMEC, *University of Luxembourg, **University of Antwerp

The scalability potential of low resistivity ternary metallic alloys (MAX) as an interconnect medium has been benchmarked against copper through first-principle simulations.

11:50 PM 12-4

A First-Principles Density Functional Theory based framework for barrier material screening, G. Hegde, R. C. Bowen, H. Simka, Advanced Logic Lab, Samsung Semiconductor Inc (SSI)

A first principles Density Functional Theory (DFT) based framework for barrier material screening is described. The vertical component of barrier resistance - a crucial component of via resistance difficult to access through experiments - is estimated by statistically averaging electron transmission from an ensemble of transport calculations in the Non-Equilibrium Greens Function (NEGF) formalism. The framework is successfully validated for the TaxNy system using datasets in the literature. Use of the framework as a first step towards predictive barrier material screening is illustrated, by comparing TaxNy with a different class of material.

12:15 pm LUNCH

Session 13 - Materials and Unit Process 3 - Metals

Session Chairs: Luke Henderson, Romy Liske

1:30 PM 13-1

Resistance Scaling of Cu Interconnect and Alternate Metal (Co, Ru) Benchmark toward sub 10nm Dimension, He Ren, Zhiyuan Wu, Nikos Bekiaris, Jennifer Tseng, Gary How, Xiangjin Xie, Wei Lei, Rong Tao, Roey Shaviv, Joung Joo Lee, Ramkumar Vinnakota, Keyvan Kashefizadeh, Max Gage, Mehul Naik, Applied Materials, Inc.

Interconnect line resistance at smaller dimension is a critical scaling roadblock. While efforts continue to manage resistance of Cu interconnect, Cu replacements such as Co, Ru are under active consideration as next generation interconnects. It is important to characterize how these metals scale with respect to each other to provide input into the technology roadmap. Here, we present our work on resistance benchmarking of Cu, Co and Ru interconnects down to less than 10nm CD to help shed light from a scaling perspective.

1:55 PM 13-2

Embedded metal voids detection to improve Copper metallization for advanced interconnect, J. Tseng, Applied Materials, Inc

We present here our studies on using electron beams to locate copper fill voids in dual damascene structures down to 10nm CD. It is shown that the e-beam technique can be optimized for detecting embedded voids in non-destructive manner that enables faster process development on 300mm wafers by reducing the dependence on time consuming methods such as Transmission Electron Microscope (TEM), while at the same time providing statistically significant information during process development and monitoring.

2:20 PM 13-3

Damascene benchmark of Ru, Co and Cu in scaled dimensions, Marleen H. van der Veen, N. Heylen, O. Varela Pedreira, I. Ciofi, S. Decoster, V. Vega Gonzalez, N. Jourdan, H. Struyf, K. Croes, C. J. Wilson, Zs. Tőkei, Imec

The alternative metals Ru and Co are benchmarked to Cu in a damascene vehicle at scaled dimensions. Ru and Co are found to be superior in line resistance for trenches smaller than 250nm2. The work is complemented with a via R modelling and EM performance comparison. Here, the barrierless Ru is superior at both levels.

2:45 pm BREAK

Session 14 - 3D Process and Integration

Session Chairs: Valeriy Sukharev, Tetsu Tanaka

3:05 PM 14-1

From direct bonding mechanism to 3D applications (Invited),

F. Fournel, H. Moriceau, V. Larrey,C. Morales, C. Mauguen, C. Bridoux
Univ. Grenoble Alpes, CEA, LETI

Nowadays Silicon direct wafer bonding is a mass production technology in many different applications. Starting around the sixties for industrial optical system elaboration, its major development is now in the microelectronic, microtechnology and optoelectronic fields. Obviously to reach such a mature level, the direct bonding mechanisms have to be established. The silicon or silicon dioxide direct bonding is now well established and direct bonding using metallic surfaces starts also to be investigated. For instance, copper or titanium direct bonding mechanism are established. The behavior of hybrid direct bonding using surfaces composed of both materials can then be understood. This hybrid bonding paves the way to high-density interconnection bonding for 3D applications.

3:35 PM 14-2

Advances in SiCN-SiCN Bonding with High Accuracy Wafer-to-Wafer (W2W) Stacking Technology,

L. Peng, S-W Kim, S. Iacovo, F. Inoue, A. Phommahaxay, E. Sleeckx, J. De Vos, D. Zinner*, T. Wagenleitner*, T. Uhrmann*, M. Wimplinger*, B. Schoenaers**, A. Stesmans**, V. V. Afanas'ev**, A. Miller1, G. Beyer1, E. Beyne1, IMEC, *EV Group, **University of Leuven

Results are presented of recent studies in material exploration for W2W bonding and advanced W2W alignment carried out as a holistic approach to enable a robust ultra-fine pitch interconnect for 3Dsystem-on-chip (SoC) technology.

4:00 PM 14-3

Novel Bonding Process Using Ultra-thin Mn for Highly Robust and Reliable Cu/SiO Hybrid Bonding,

K. Uchida, K. Tsumura, K. Nakamura, K. Higashi, Y. Sugizaki, H. Shibata, Toshiba Corporation

We suggest a new Cu/SiO hybrid bonding process using ultra-thin Mn film at the bonding interface. In this process, bonding stability can be improved because bonding interface consists of only Mn. In addition,Mn on SiO forms MnSiO dielectric known as diffusion barrier for Cu during thermal process, results in improving the reliability of interconnects at misalignment area. In order to prove the possibility of this process, we evaluated bonding strength of Mn/Mn interface and electric property of oxidized Mn film. Good bonding strength was obtained at the condition of annealing at 350°C or more temperature. Moreover, it was confirmed that the resistivity of ultra-thin Mn film on SiO layer was increased by heat treatment.

4:25 PM 14-4

3D packaging+Cooling --- "Beat the heat in 3D Chip stacks with Novel microfluidics" (Invited),

T. Chainer, **P. R. Parida**, M. Schultz, F. Yang, M. Gaynes, G. McVicker, A. Sridhar, S. Paredes, O. Ozsun, T. Brunschwiler, U. Drechsler, E. Colgan, B. Dang, Y. Liu, Q. Chen, A. Buyuktosunoglu, A. Vega, Y. Kwark, L. Shan, D. Liu, J. Silbermann, B. Webb, R. Joshi, J. Knickerbocker, C. Tyberg
IBM

In the Moore's Law race to keep improving computer performance, the IT industry has turned upward, stacking chips into skyscrapers. The 3D chip stacking technology has the potential to enable increased system performance through close integration of heterogeneous system components such as accelerators and/or high-density memory. However, 3D chips stacks, like the law they are challenging, have limits due to heat generation. A solution to remove the heat in 3D stacks is embedded cooling in which a benign

nonconductive dielectric fluid (like the one used in refrigeration systems) is made to flow through microscopic gaps, some no wider than a single strand of hair (~100 μm), between the stacked high power active layers [1-2]. This dielectric fluid can come into contact with electrical connections, so is not limited to one part of a chip or stack. The fluid is pumped into the chips, where it removes the heat from the chip by boiling from liquid-phase to vapor-phase. The vapor is then condensed back to liquid and recirculated. This two-phase cooling technology not only delivers a lower device junction temperature (Tj), but also reduces system size, weight, and power consumption [3-5].

4:55 pm
Sessions end