Monday, June 4

Selective Deposition Workshop

Workshop Chairs: Larry Zhao, Terry Spooner

8:15 am
Welcome and Introductions

8:30 am
Selective Deposition Challenges and Opportunities for Patterning, Efrain Altamirano-Sanchez

9:20 am
Selective Metal CVD and Nano Fabrication Applications, Son Van Nguyen

10:10 am
BREAK

10:40 am
Selective Processes: Challenges and Opportunities in Semiconductor Scaling, Kandabara Tapily

11:30 am
Substrate-selective Reactions in Atomic Layer Deposition and Atomic Layer Etching, Greg Parsons

12:20 pm
LUNCH

1:20 pm
Area and Topographical Selectivity in Atomic Layer Deposition, Stacey Brent

2:10 pm
Precursor and Inhibitor Design for Selective ALD/CVD, Jean-Marc Girard

3:00 pm
BREAK

3:30 pm
A Tutorial on Electrochemical Atomic Layer Deposition: How Electrochemistry Enables Atomically-Precise and Selective Deposition of Metals, Rohan Akolkar

4:10 pm
Selective Electroless Deposition: Process, Challenges, and Solutions and its Critical Role in RC Scaling, Artur Kolics

5:10 pm
WORKSHOP ENDS

Tuesday, June 5

Session 1 – Keynote Session

8:15 am
Welcome, Introduction and Awards, Noel Russell, TEL, General Chairman

8:25 am
Keynote Presentation
The Viability of Quantum Computing from an Interconnects Perspective, James S. Clarke, Intel Corporation

Quantum computing is an emerging compute technology that holds the promise of exponential speedup compared to classical computing for certain applications. Relatively small numbers of logical quantum bits, or qubits, could outperform the largest of supercomputers. For many universities, companies, and governments, this is akin to a modern space race or moon shot. Applications in the areas of chemistry, medicine, machine learning, and cryptography may be enabled with quantum computers where a classical computer could not accomplish the task on any realistic timescale.

Two of the most promising qubit technologies are superconducting qubits and spin qubits in silicon. These technologies bare similarities to the device and interconnect technologies used in advanced CMOS processing today. Examples are shown below. Intel's Tangle Lake 49-qubit superconducting chip is shown on the left while our first 3-qubit spin system is shown on the right. At present, the quantum community is exploring systems comprised of a few 10's of qubits with a long term goal of several million on a single chip. What is the bottleneck to moving beyond few-qubit devices? In a word... Interconnects! Today's qubits have personalities. They are all different. Individual control of each qubit is required, which puts pressure on interconnect topologies and control electronics.

In this talk, we'll introduce the key concepts of quantum computing. Then we'll show the building blocks of the quantum computer including the materials and devices required to operate qubits at temperatures near absolute zero. Finally, we'll talk about the key challenges to go from the few qubit regime to a commercial scale system.

9:15 am
BREAK

Session 2 - Process Integration 1

Session Chairs: Dan Edelstein, Andrew Yeoh

9:35 am 2-1
The Future of Interconnects: Challenges and Enabling Technologies (Invited), Kevin Lin, Manish Chandhok, Miriam Reshotko, Intel Corporation

Enabling resistance and capacitance scaling are key to delivering interconnect performance for future technology nodes [1]. Copper interconnects become less advantageous at smaller dimensions due to the large mean free path of Copper and the need for a diffusion barrier. In addition, electromigration (EM) limits the current density of copper interconnects at small dimensions [2]. Novel barriers for copper may be used to increase the copper volume fraction of an interconnect line, and alternate metals with shorter mean-free-paths (MFP) may offer barrier-free solutions for future technology nodes [3]. To improve capacitance, carbon-doped silicon dioxides (CDO) has been implemented in modern technologies [1]. However, it has been difficult to integrate porous low-K inter-layer dielectrics (ILD) into interconnect systems [1]. This talk

presents opportunities with using pore stuffing to improve patterning to enable low-K integration [4, 5] and the simulated capacitance and performance benefits using pore stuffing technologies.

As interconnect line patterns formed from gratings, pitch-division solutions exist to make interconnect lines that are smaller than the minimum resolvable pitch from lithographic patterning; however, it has become increasingly difficult to print cuts and vias [6, 7]. Existing approaches require multiple passes of cuts and vias, which not only increases the cost, but makes alignment more challenging [6, 7]. In addition, edge placement error (EPE) from various sources such as registration errors, line edge roughness, and critical dimension (CD) variation becomes increasingly important at smaller dimensions [6, 7, 8]. One solution to mitigate via shorting to the wrong line by using hard masks of different materials with high etch selectivity [9]. This talk details the benefits of via shorting improvement through different hard masks, given edge placement error assumptions. Furthermore, using selective deposition may enable self-alignment techniques to reduce total EPE [10].

The overall BEOL interconnect solution is becoming increasingly integrated. Metallization, dielectric, and patterning are challenges have important interdependencies so the interconnect solution needs to be co-optimized. These solutions will be enabled with the advent of new materials and innovative patterning techniques.

10:05 AM 2-2

High-Aspect-Ratio Ruthenium Lines for Buried Power Rail, Anshul Gupta, Shreya Kundu, Lieve Teugels, Jürgen Bömmels, Christoph Adelmann, Nancy Heylen, Geraldine Jamieson, Olalla Varela Pedreira, Ivan Ciofi, Bharani Chava, Christopher J. Wilson, Zsolt Tőkei, Imec

High-aspect-ratio (HAR) Ru power rails, buried in front-end-of-line (FEOL) oxide, can potentially replace conventional middle-end-of-line (MOL) Cu power rails. The HAR feature can boost performance by reducing resistance and voltage drop along the power line. The buried nature, helps to minimize standard cell height by freeing up routing resources at MOL, enabling overall area scaling. This paper demonstrates, Ru lines of aspect ratio up to 7, at a CD of 18 nm. Line resistance at these dimensions, measures at 60 Ω/μm, with the minimum electrical resistivity of 8.8 μΩcm, as extracted from the temperature-controlled-resistance (TCR) measurements. HAR Ru lines are also found to withstand very high FEOL thermal budgets, such as 1000 °C activation anneal for 1.5 s. The combination of all these factors, make HAR Ru buried power rail, a promising scaling booster for next generation technology nodes.

10:30 AM 2-3

Electroless Cobalt Via Pre-Fill Process for Advanced BEOL Metallization and Via Resistance Variation Reduction, J. Gu, D. Zhao, M. Kamon, D. M. Fried, G. Harm*, T. Mountsier*, Coventor, Inc, a Lam Research Company, *Lam Research

While processes have been developed to reduce nominal via resistance due to resistive Ta/TaN barrier layers, little effort has been made to show improvements to counteract the shrinking process window for via resistance with technology dimension. An electroless Co via-prefill process can improve nominal resistance, and in this paper, we quantitatively demonstrate improvement in process variability. Through process modeling with virtual fabrication, we also scale this prediction to 7 nm where the variability of the typical Ta/TaN approach is 50% higher with Co via-prefill.

10:55 AM 2-4
Subtractive Etch of Ruthenium for Sub-5nm Interconnect, D. Wan, S. Paolillo, N. Rassoul, B. K. Kotowska, V. Blanco, C. Adelmann, F. Lazzarino, M. Ercken, G. Murdoch, J. Bömmels, C. J. Wilson, and Zs. Tőkei, imec

Ruthenium has been considered to replace copper in advanced nodes. We fabricated Ru structures using EUV and subtractive etch. Lines with CD<10.5 nm were formed and tested. Using TCR method, resistivities and areas were obtained. Ru lines with AR 3.8 were fabricated and have resistance below 500Ω/μm at 12 nm CD. Ru is expected to outperform damascene Cu at this scale, supporting insertion of subtractive etch Ru for advanced technology nodes.

11:20 AM 2-5
Impact of liner metals on copper resistivity at beyond 7nm dimensions, H. Huang, N. Lanzillo, T. E, Standaert, K. Motoyama, C. Yang, H. Shobha, J. Maniscalco, T. Nogami, J. Li, T. Spooner, G. Bonilla, IBM

The impacts of ruthenium and cobalt liners on copper resistivity have been investigated at beyond 7nm dimensions. Liner metal conduction was carefully evaluated in a Cu resistivity derivation using the temperature coefficient of resistivity (TCR) approach. Cu resistivity with Ru liner is higher than with a Co liner by 10-15%, which is verified by RC plot. The resistivity difference is attributed to interface scattering and possibly grain boundary scattering. Interface ab initio calculations show 3-7% increase of Cu resistivity from Coliner to Ru liner.

11:45 pm
LUNCH

Session 3 - Novel Interconnect Materials and Systems

Session Chairs: Fabrice Nemouchi, Mansour Moinpour

1:00 PM 3-1
Challenges and Progress on Carbon Nanotube Integration for BEOL Interconnects (Invited),
B. Uhlig[1], A. Dhavamani[1], N. Nagy[1], K. Lilienthal[1], R. Liske[1], R. Ramos[2], J. Dijon[2], H. Okuno[3], D. Kalita[3], J. Lee[4], V. Georgiev[4], A. Asenov[4], S. Amoroso[5], L. Wang[5], F. Koenemann[6], B. Gotsmann[6], G. Goncalves[7], B. Chen[7], J. Liang[8] , R. R. Pandey[8], R. Chen[8], A. Todri-Sanial[8], [1]Fraunhofer IPMS, Dresden, Germany; [2]CEA-LITEN/University Grenoble Alpes, France; [3]CEA-INAC/University Grenoble Alpes, France; [4]School of Engineering, University of Glasgow, UK; [5]Synopsys Inc., Glasgow, UK; [6]IBM Research Zurich, Switzerland; [7]Aixtron Ltd., UK; [8]CNRS/LIRMM-University of Montpellier, France

Here, we review and present current challenges and progress on Carbon Nanotube Integration for BEOL Interconnects as well as our recent results. Amongst all the research on carbon nanotube interconnects, those discussed here cover 1) improvement of the variability of SWCNTs for local interconnects 2) process & growth of carbon nanotube interconnects compatible with BEOL integration and formation of CNT-copper-composites, 3) modeling and simulation from atomistic to circuit-level benchmarking and performance prediction, and 4) characterization and electrical measurements. The aim is to evaluate the use of CNT-based materials for future metallization, both in regards to manufacturability, i.e. CMOS compatibility and wafer-scale integration as well as realistic performance expectations, i.e. variability and defectivity.

1:30 PM 3-2
CMOS-Compatible Contacts for Si Photonics From Solid-State Reaction to Laser Integration, E. Ghegin* **, S. Zhiou**, S. Bensalem**, L. Toselli**, M. Pasquali**, S. Favier* **, C. Jany **, B. Szelag**, P. Gergaud**, F. Nemouchi**, Ph. Rodriguez**, * STMicroelectronics, ** CEA LETI

From surface preparation and solid-state reaction to laser integration, a short overview of the CMOS compatible contacts developed in our group on n-InP and p-InGaAs for Si photonic applications is proposed.

1:55 PM 3-3
Single Crystal Al Interconnects Formed on p-GaN and Their Application to GaN FET, Takeshi Harada, Koji Utaka, Yusuke Kanda, Katsuhiko Onishi,Keiichi Matsunaga*, Masahiro Hikita*, Yasuhiro Uemoto*, Panasonic Semiconductor Solutions, *Panasonic

A new technology for manufacturing GaN FET is proposed. A Ti/Al/Ti stackcontacting to p-GaN is used as a gate metal. Surprisingly, Al forms a single crystal. It is due to an epitaxial growth of Al on p-GaN. Sheet resistance of the Ti/Al/Ti stack is decreased by the single crystal formation. Electromigration lifetime is drastically improved with the fraction of the single crystal. In addition, the Ti/Al/Ti stack shows very low contact resistance to p-GaN.

2:20 PM 3-4
Graphene Interconnects – High Performance Twisted 20 nm Graphene Ribbons, X. Wu, A. Contino, B. Soree, M. Heyns, I. Asselberghs*, C. Huyghebaert*, Z. Tokei*, KU Leuven, *IMEC

We investigate the effect of interlayer coupling on the electrical performance of few layer graphene (FLG) interconnects. On SiO2, AB-stacked graphene layers show low carrier mobility due to strong interlayer coupling and formation of parabolic bands. A dramatic increase in carrier mobility and conductivity is observed when the graphene layers are twisted. At sufficiently large angles, single layer graphene (SLG) like behavior is observed in the FLG. Furthermore, the electrical resistance of scaled ribbons down to 20nm width and possible failure mechanisms in graphene wires is investigated. Record values up to 2000cm2/Vs are reported for scaled FLG ribbons below 100nm.

2:45 pm
BREAK

Session 4 - Contacts and Local Interconnects

Session Chairs: Paul Besser, John Zhu

3:05 PM 4-1
Contact Metallization for Advanced CMOS Technology Nodes (Invited), **V. Kamineni**, A. Carr*, C. Niu, P. Adusumilli*, T. Abrams, R. Xie, S. Fan*, J. Kelly*, H. Amanapu*, S. Tsai, K. Ryan, Y. Liang, X. Lin, S. Choi*, H. Dixit, A. Konar, N. Lanzillo*, H. Wu*, J. Cho, D. Guo*, K. Choi*, M. V. Raymond, GLOBALFOUNDRIES Inc.;*IBM

Continuous CMOS scaling is being driven by innovation of novel device architectures to improve device performances at lower power consumption [1]. However, middle-of-the-line (MOL) continues to be a key performance and yield detractor for scaling. To alleviate these challenges, disruptive MOL architectures and materials are being proposed. At the ≤ 10NM node, significant differences are already seen in the MOL architecture and materials used by leading semiconductor companies [2-4]. This is expected to continue to smaller CMOS nodes where contacts represent significant contribution to external resistance (Rext). Figure 1 illustrates the impact of scaling on source/drain (S/D) contact vertical resistance, which can be quantified as the sum of silicide contact resistance (RC) and trench metallization resistance (RTS) [5]. It can be

observed that at ≥ 20 nm trench bottom critical dimension (BCD), silicide contact resistance is the predominant contributor to the total vertical resistance. At these dimensions, it is critical to lower the specific contact resistivity (ρC) to reduce the vertical resistance. At narrow (< 20 nm) dimensions, it is observed that trench metallization resistance (for ρC = 0) contribution to the total vertical resistance starts to increase. In addition, below ~11nm of BCD we see an inflection in resistance because of the change in transport from high resistive nucleation layers to liner/barrier materials. It should be noted that this figure was generated using resistance calculations for a simple trench dimension not specific to any technology and typical MOL materials.

3:35 PM 4-2
Extreme Contact Scaling with Advanced Metallization of Cobalt, Raymond Hung, Jin Hee Park, Tae Hong Ha, Mark Lee, Wenting Hou, Jianxin Lei, Jonathan R. Bakke, Shashank Sharma, Karthik Raman Sharma1, Amir Wachs*, Nam Sung Kim, Ellie Yeh, Applied Materials Inc., Sunnyvale, CA, USA, *Applied Materials Israel, Rehovot, I

Extending tungsten contact for the most advanced nodes (≤ 7 nm) is challenging due to the growing impact of contact resistance on the overall resistance of a device and to the increasing difficulty of gapfill in features with < 20 nm critical dimensions. The paper presents a gapfill material using metal-organic chemical vapor deposition (MO-CVD) cobalt for contact plug.Highlights of new gapfill material include proven seamless, voidless gapfill and contact resistance reduction. CVD Cobalt anneal parameters are discussed that can be optimized in combination with the deposition process to achieve desired gapfill. A proprietary electron-beam imaging technology was used to qualify the cobalt fill for void-free performance. Various process flows are discussed that lead to the best-known fill and resistance reduction values.

4:00 PM 4-3
Replacement Metal Contact Using Sacrificial ILD0 for Wrap Around Contact in Scaled FinFET Technology, S-A. Chew, S. Demuynck, L. Zhang, A. Pacco, K. Devriendt, L. Teugels, T. Hopf, J. Versluijs, C. Vrancken, A. Dangol, E. Altamirano Sanchez, D. Mocuta and N. Horiguchi , Imec, Leuven, Belgium

In this work, we propose replacement metal contact (RMC) flow by using sacrificial ILD0 that is suitable for wrap around contact (WAC). RMC minimize erosion of gate plug, spacer and Source/Drain area at scaled contact formation. The concept of the flow has been demonstrated in short loop flow with ~50% contact resistance improvement for both NMOS, Si:P and PMOS, SiGe:B.

4:25 PM 4-4
Validity and Application of the TCR Method to MOL Contacts, E. Milosevic, V. Kamineni*, X. Zhang**, H. Dixit*, H. Huang***, R. Southwick***, C. Janicki***, N. Lanzillo***, D. Gall, M. V. Raymond* Rensselaer Polytechnic Institute, *GLOBALFOUNDRIES Inc., **Cisco Systems Inc., ***IBM Research

As structure size decreases, electron scattering and liner conduction effects may lead to inaccuracy in the TCR method. To investigate these potential issues for tungsten systems, resistivity, grain size, and temperature derivatives of sheet resistance are measured as a function of thickness for CVD deposited films. Liner conduction was found to impact the apparent temperature dependence of sheet resistance for thin W films. W films exhibit a dρ/dT value 39% higher than reported in literature for bulk. The effect of electron scattering at surfaces and grain boundaries on the temperature derivative of sheet resistance is predicted from common classical scattering models and it is concluded that these mechanisms do not play a significant role. It was also found that TCR accuracy is improved in W contact structures by using the derivative of resistivity determined from the W blanket film analysis. In addition, we also calculated TCR values from first principles which are in good agreement to our experimental results.

4:50 pm Sessions end

Wednesday, June 6

Session 5 - Keynote

Session Chair: Todd Ryan

8:15 am

CMOS/Cu BEOL Technology in Manufacturing: 20 years and Counting, Dan Edelstein, IBM

This keynote speech will recount some key innovations, anecdotes, and milestones associated with the development and implementation of Cu BEOL into CMOS manufacturing 20 years ago, and carry this discussion through its evolution to the present time, and its future prospects.

Last year marked the 20th anniversary of IBM's industry-first CMOS/Cu BEOL technology to reach early production. The subsequent manufacturing volume-ramp in mid-1998 provided the first market for CMOS CPU and other high-performance logic chips with Cu BEOL. The salient features of the original technology definition that was implemented here have largely endured to the present day, though with steady evolutionary improvements. These original features included multilevel Cu dual damascene integration, a TaN/Ta bilayer liner, PVD Cu-seed with electroplated Cu fill, 2-step CMP, a PECVD Si3N4 barrier cap with NH3-based plasma preclean, and SiO2 interlevel dielectric. As well, architectural features enabled by Cu damascene included large-range plane-pair hierarchical wire scaling, from low-C/high-density/short-length fine levels to low-R/long-length global levels, and Al-based transitions to wirebond and C4 terminals. With proper integration techniques with these materials and interfaces, we were able to realize Cu's promise of many orders of magnitude longer electromigration lifetimes than the Al(0.5%Cu) alloy that it replaced. This last aspect has fundamentally kept Moore's Law scaling alive for the BEOL wiring, which would otherwise have broken with Al(Cu) long ago.

Now in its 10th generation of CMOS manufacturing, and 12th generation in the research phase, we are finally starting to see changes beyond evolutionary in the materials and processes, with the end in sight for the Cu finest wires in perhaps 1-2 more generations. However, our current data for recent innovations still suggests this Cu/alternate metal crossover point may be pushed off at least once more beyond some predictions.

Session 6 - Process Integration 2

Session Chairs: Susumu Matsumoto, Hui Jae Yoo

9:05 AM 6-1

Ru liner scaling with ALD TaN barrier process for low resistance 7 nm Cu interconnects and beyond, K. Motoyama, O. van der Straten, J. Maniscalco, H. Huang, YB. Kim*, JK. Choi*, JH. Lee*, C.-K. Hu, P. McLaughlin, T. Standaert, R. Quon, and G. Bonilla, IBM Research, *Samsung Electronics Co. LTD.

Low resistance Cu interconnects with CVD Ru liner have been demonstrated for 7 nm node. Ru liner thickness reduction has been achieved by replacing PVD TaN with a bilayer PVD Ta and ALD TaN stack, while maintaining adequate Cu fill performance. The newly proposed barrier stack (PVD Ta/ALD TaN) with thin Ruliner studied in this paper also enabled a significant Ru CMP performance improvement by mitigating two major Ru CMP issues: Cu recess of narrow lines, and trench height variability between dense and isolated patterns. Furthermore, this novel barrier stack with Ru liner could attain void-free Cu fill even for beyond 7 nm node dimension. Thus, the PVD Ta/ALD TaN/CVD Ru liner is a promising candidate as the liner for Cu interconnects of 7 nm node and beyond.

9:30 AM 6-2

Modified ALD TaN Barrier with Ru Liner and Dynamic Cu Reflow for 36nm Pitch Interconnect Integration, P. Bhosale, J. Maniscalco, N. Lanzillo, T. Nogami, D. Canaperi, K. Motoyama, H. Huang, P. McLaughin, R. Shaviv*, M. Stolfi*, R. Vinnakota*, G. How*, S. Pethe*, b. Sheu*, x. Xie*, L. Chen*, IBM Research, *Applied Materials

Integration of thermal atomic layer deposition (ALD) TaN films modified by physical vapor deposition post-treatment (PPT) and in-situ plasma treatment (IPT) was investigated on 36nm pitch BEOL structures. The PPT and IPT processes produce an interface more suitable for liner (Co/Ru) and physical vapor deposition (PVD) of Cu seed. This results in improvement in Cu gap-fill for both traditional Cu seed/plating process with 15 Å chemical vapor deposition (CVD) Co liner and dynamic PVD Cu reflow (DCR) on 20 Å CVD Ru liner. The PPT also decreased via resistance (R) by sputtering TaN at bottom of the via. IPT processes densify the ALD films and improve EM performance. A promising integration scheme of 20 Å ALD+IPT TaN/20Å Ru/DCR was developed with 20X improvement in electromigration.

9:55 am BREAK

Session 7 - Reliability

Session Chairs: Roey Shaviv, Kazuhoshi Ueno

10:15 AM 7-1

Microstructure Evolution and Implications for Cu Nanointerconnects and Beyond

Szu-Tung Hu[1], Linjun Cao[2], Laura Spinella[3] and **Paul S. Ho**[1], [1]The University of Texas at Austin; [2]GLOBALFOUNDRIES; [3]National Renewable Energy Laboratory

The continued scaling of Cu low k technology is facing serious challenges imposed by basic limits from materials, processing and reliability. This has generated great interests recently to further develop Cu nanointerconnects and alternates, particularly Co and Ru nanointerconnects beyond the 10nm node. The performance and reliability are important considerations for the development of nanointerconnects in addition to challenges from processing complexity and manufacturing cost. In this paper, we investigate the microstructure evolution in Cu, Co and Ru nanointerconnects and the effects on resistivity and electromigration (EM), two key factors contributing to the RC delay and reliability of the nanointerconnects.

The scaling effect on microstructure of Cu interconnects was analyzed down to the 24 nm linewidth for the 14 nm node using a TEM-based high-resolution diffraction technique with capabilities to map in detail the orientation and size distribution of individual grains [1]. The TEM observation was supplemented by a Monte Carlo simulation for grain growth based on local energy minimization, taking into account orientation-dependent grain boundary, strain, and interface energies in order to examine the effect of scaling and material properties on grain growth [2, 3]. The results of this study revealed a consistent picture of microstructure evolution with scaling in Cu nanointerconnects. With the linewidth exceeding 180 nm, a dominant growth of the (111) grains which have the lowest grain boundary energy was observed from the trench bottom, a process controlled by the interface energy. As scaling reduces the linewidth to 120 nm, the growth of the (111) grains began to shift to the trench sidewalls, reflecting the change in the aspect ratio but still interface energy controlled. Twin boundaries were readily observed although only a small fraction being the Σ3 coherent boundaries, which is induced by the strain energy during annealing converting some (111) to (200) grains in order to minimize the elastic anisotropy of Cu. The amount of twin boundaries continued to decrease with scaling and reached to ~1% at 70nm linewidth while small grains emerged near the trench bottom. With further scaling to the 45 nm linewidth (28 nm node), the growth of (111) grains shifted again to along the trench length direction, a trend which continued to the 22 nm linewidth with the appearance of more small grain aggregates, indicating further dominance of the interface energy in comparison to the strain energy with increasing surface to volume ratios.

The result of the microstructure study was used to analyze the scaling effect on the resistivity of Cu nanointerconnects and EM lifetime. We are able to account for the scaling effect on resistivity from the contributions of surface and grain boundary scatterings as reported in a recent study [4]. The scaling effect on EM lifetime was analyzed based on a recent study reporting excellent lifetime and high (1.5-1.6eV) activation energy for the 24 nm Co-capped Cu nanointerconnects [5]. We found that based on the microstructure of the 24 nm Cu nanolines, this will require the Cu grain boundaries to be de-activated, perhaps by "stuffing" with Co atoms as observed in the EM study. Finally, microstructure evolution studies were carried out for Co and Ru by simulation and some limited TEM observations. Results will be reported together with model analyses of the scaling effect on Co and Ru resistivity and electromigration.

10:45 AM 7-2

Electromigration and Thermal Storage study of Barrierless Co vias, O. Varela Pedreira, K.Croes, H. Zahedmanesh, K. Vandersmissen, M. H. van der Veen, V. Vega Gonzalez, D. Dictus*, L. Zhao**, A. Kolics**, Zs.Tőkei, Imec vzw, *Lam Research Belgium, *Lam Research Corp. Fremont, CA

We study the reliability performance in terms of electromigration and thermal storage of barrierless Co vias. While for our reference with Cu filled vias and a TaNCo barrier/liner system we did observe voids in some vias after electromigration, these voids were not observed for the Co vias and thus the studied system is more scalable towards smaller vias. Long thermal storage measurements show more failures in barrierless Co vias. As this problem is linked to a weak Co/dielectric interface and Co/Cu-intermixing, a better adhesion between the Co and the low-k, the use of a non-porous low-k dielectric and the use of a barrier at the via bottom could help to reduce this phenomenon.

11:10 AM 7-3

Pathfinding of Ru-Liner/Cu-Reflow Interconnect Reliability Solution, Z. Wu, F. Chen, G. Shen, Y. Hu, S. Pethe, J. J. Lee, J. Tseng, W. Suen, R. Vinnakota, K. Kashefizadeh, M. Naik, Applied Materials, Inc.

Ruthenium (Ru) and Copper (Cu) interface promotes void-free Cu gap-fill through a Cu reflow approach. However, reliability issues such as Electromigration (EM) and time-dependent dielectric breakdown (TDDB) have delayed industry adoption of Ru liner. Here, we report our findings on two EM improvement approaches and compare them to industry standard Cobalt (Co) liner/selective Co cap based Cu interconnect. Similar to Co liner, addition of a post chemical mechanical planarization (CMP) selective Co cap did improve EM performance with Ru liner. However, EM equivalence to Co liner/Co cap based Cu interconnect requires the development of a new doped Ru liner in combination with the selective Co cap. We will also discuss the impact of the EM improvement approaches on key parameters of interest such as via resistance, TDDB and provide a technology scorecard.

11:35 PM 7-4

Testing The Limits of TaN Barrier Scaling, C. Witt, K.B. Yeap, A.Lesniewska*, D.Wan*, N.Jordan*, I.Ciofi*, C. Wu*, Z. Tokei*, GLOBALFOUNDRIES, *IMEC

The thickness limit of PVD TaN diffusion barrier plus either Co or Ru liner was studied by TDDB testing. A special planar metal-insulator capacitor has been used for this purpose. The TaN range was 0.2 to 3nm, deposited by a low power PVD process. It is found that both Co and Ru liners can add significantly to the barrier integrity. TaN can be thinned to <0.8nm in conjunction with Co. The combination of TaN and Ru showed excellent barrier properties, with TaN as thin as 0.5nm. The impact on line and via resistance is being discussed.

12:00 pm LUNCH

Session 8 - Materials and Unit Process 1 - Dielectrics

Session Chairs: Bryan Hendrix, Tatsuya Usami

1:15 PM 8-1

ALD/Surface functionalization for Conductivity (Invited), Han Bo Ram Lee, Incheon National University

Atomic layer deposition (ALD) is a thin film deposition method employing self-saturated surface reactions. Since ALD has several superior properties for nanoscale device fabrications, such as excellent conformality, large area uniformity, and process compatibility over the conventional thin film deposition methods, it has been widely applied for various high technology applications from semiconductor to display devices. Due to the surface reaction mechanism, ALD can be an effect route to change and modify surface properties with precise controllability in other applications. In this work, we utilized ALD as a tool for surface property modification, in particular, two examples were introduced, improvement conductivity of graphene and organic textiles. Ideally, graphene has high conductivity due to its unique atomic structure, however, it is not achievable in real system because of inevitable formation of defects during synthesis process which deteriorates the conductivity. Pt was selectively formed on the defect sites of chemically-synthesized graphene layer by ALD to improve the low conductivity of graphene, and Pt-decorated graphene was applied to transparent conducting heater system. Fabrication of conductive textiles is important to enable wearable electronics. Inspired from the conventional dyeing technology, we coat textiles with ALD Pt and Ru through organic-inorganic hybridization in atomic level. A capacitive type pressure sensor was fabricated by using the highly conductive ALD-modified textile fibers, and applied to seat sensor for vehicle. The ideas in these two examples could be also applied to other applications which require surface modifications and conductivity improvement without significant change of original properties.

1:45 pm 8-2

Nonaffine Deformations in ULK Dielectric Glasses, K.I. Kilic, R. H. Dauskardt, Stanford University

Our manuscript points out for the first time to the relation between small scale deformation characteristics of ULK dielectric glasses and their mechanical properties. This is a crucial result in the sense that it provides an insight towards which molecular level parameters are controlling thestiffness of ULK organosilicate glasses. Revelation of the connection between deformation characteristics and mechanical properties is a strong step towards designing mechanically more robust and reliable ULK dielectric glasses.

2:10 pm 8-3

Effect of thermal annealing on low-k dielectrics for iBEOL in view of 3D sequential integration, S. Beaurepaire, V. Jousseaume, P. Gonon*, A. Bsiesy*, C. Guérin, N. Rochat, C. Licitra, P-L. Charvet, M. Veillerot, N. Rambal, D. Nouguier**, D. Ney**, X. Federspiel**, C. Fenouillet-Béranger, CEA-Léti, *LTM-UGA, **STMicroelectronics

This work presents an in-depth study of the thermal stability of low-k material in view of intermediate Back-End-Of-Line (iBEOL) for 3D sequential Integration. SiOCH ULK were analyzed after thermal annealing up to 600°C. Moreover, the stability and reliability of this ULK material coupled with W metal in line 1 integration is characterized up to 550°C, 5h. We have demonstrated that low-k material can support a thermal budget of 500°C, 2h with limited outgassing. This result is fully compatible with 3D sequential integration.

2:35 pm
BREAK

Session 9 - Design/Technology Co-optimization

Session Chairs: Mehul Naik, Xiaopeng Xu

2:55 PM 9-1

BEOL Layout Design Considerations To Mitigate CPI Risk (Invited), **Mohamed A. Rabie**, Thiagarajan Raman, Fahad Mirza, Nicholas A. Polomoff, Danish Faruqui, Scott Pozder, Md Khaled Hassan, Tamer Desouky, and Carole Graas, GLOBALFOUNDRIES

We present a summary of some of the main Back End of Line (BEoL) design optimization techniques to mitigate Chip Package Interaction (CPI) risk in flip-chip configuration. Optimization techniques include metal tiles right on top of the metal stack at the corner of the die beyond the bumps, diagonal final aluminum cap metal lines under the corner bumps, octagon shape of the pads under the bumps, 80^{o} PSPI angle opening, as well as wider double rail crackstops.

3:25 PM 9-2

System-level impact of interconnect line-edge roughness, R. Baert, I. Ciofi, Ph. Roussel, L. Mattii*, P. Debacker, Zs. Tokei, IMEC, *Braunschweig University of Technology

This paper provides an analysis of the impact of LER from wire resistance to system-level performance. Our silicon-calibrated resistance model is extended to include the effect of both LER standard deviation and correlation length. The new resistance model is validated against simulations after process emulation. A CPU design is used as benchmark to assess system-level impact by propagating the wire resistance probabilities through the timing analysis to obtain a critical-path timing distribution. Results show that while there is a significant impact of LER on the resistance distribution for short wires, the effect largely averages out on system level.

3:50 PM 9-3

Impact of Line and Via Resistance on Device Performance at the 5nm Gate All Around Node and Beyond, N. Lanzillo, K. Motoyama, T. Hook, L. Clevenger, IBM

This work explores the impacts of line and via resistance on overall device performance (delay, frequency vs. power) across several past and future technology nodes, including 7nm, 5nm and 3nm. This multi-scale approach employs ab initio calculations of via resistance, finite-element calculations of line resistance, and performance modeling taking into account BEOL parasitics.

4:15 PM 9-4

Interconnect-device co-optimization for field-effect transistors with two-dimensional materials, D.Verreck, G.Arutchelvan*, I.Ciofi, M.M.Heyns*, I.P.Radu, imec, *KU Leuven

The interconnect load is often disregarded in the optimization of exploratory device technologies such as field-effect transistors (FETs) with two-dimensional materials (2D). Here, we therefore combine a calibrated device model for bilayer MoS2 FETs with a three-level Cu-TaN/Ru interconnect scheme to show that the highly resistive nature of 2D FETs requires a significant decrease in wire dimensions from the nominal N5 values to achieve optimal delay. We compare a single to a double gate configuration and find the improved drive in the latter results in a lower delay at slightly increased power. In the presence of spacer regions, the extra gate also prevents a dramatic delay increase. Finally, we project that material and contacting improvements allow for a relaxation in wire dimensions.

Session 10

4:40 pm - Poster Session and Reception

10.1

Tungsten Plug Missing Defects Monitoring Method and Its Solution by Optimization of Polymer Cleaning and Micro-environment, Rongwei Fan*, Hunglin Chen, Kai Wang, Yin Long, Qiliang Ni,Shanghai Huali Microelectronics Corporation

This paper describes the tungsten (W) missing defects monitoring method with electron-beam inspection systems, and its solution by optimization of polymer cleaning and micro-environment. W missing defects detection and monitoring method was developed and fixed on bare silicon wafer. Then a series of experiments was carried out, and W missing defects were fixed by the optimization of polymer cleaning and micro-environment of the front side open unit port (FOUP).

10.2

Silicon Trench Etch Uniformity Improvement for Microloading and Macro-to-Macro Loading for sub-14nm Node, Y. Yang, S. Lim, J. Hong, M. Park, Y. Yang, W. Cho, C. Adams, M. Aminpur, and C. Maeng, GLOBALFOUNDRIES

We report a test and demonstration of plasma etching conditions that can be applied in advanced nodes beyond 14nm patterning to relieve trench depth sensitivity to incoming CD variations caused by multipatterning and macro-to-macro loading impacts from pattern density. Our result showed that lower RF duty cycle, higher bias voltage, and higher etchant flow can reduce 50% of the depth variation to incoming CD variations caused by multipatterning in previous steps and 75% of the depth differences between dense and isolated pattern areas for macro-to-macro loading.

10.3

Modulation of Within-wafer and Within-die Topography for Damascene Copper in Advanced Technology, W.-T. Tseng, T.-J. Cheng, S. Ahmed, J. Lee, F. Baumann, GLOBALFOUNDRIES

A novel copper electroplating and CMP process was developed to effectively modulate the within-wafer and within-die nanoscale topography. The feasibility of this new metallization is demonstrated on a 64nm pitch product with an equivalent defect level, lower and tighter distribution in resistance and trench height. It's believed to be extendable to other advanced nodes for a sizable reduction in copper overburden which saves CMP polish cycle time from the plan-of-record time.

10.4

The impact of solute segregation on grain boundaries in dilute Cu alloys, Takanori Tsurumaru, Luke Prestowitz*, Brendan O'Brien* and Kathleen Dunn*, SUMCO Corporation/State University of New York Polytechnic Institute, *State University of New York Polytechnic Institute

Alloying copper with cobalt may offer a means for stabilizing grain boundaries against electromigration void formation in advanced interconnects. Here we present a means for co-depositing dilute copper alloys, using Co and Ag as the solutes of interest. Microstructure and compositional analysis are presented.

10.5
Modeling wafer bending effects on RDL layer reliability in a multiple die package, Tzu Chen Wang, Chih Chieh Yeh, Xiaopeng Xu, Karim El Sayed, Chun-Hung Steven Lin*, Synopsys Inc., *Corning Display Technologies

Wafer bending effects on re-distribution layer (RDL) reliability in a multiple die package is examined using multiscale TCAD sub-modeling techniques. At the global scale, the wafer package with 200 dies and 3 RDL layers is analyzed with smear material representation. At the die scale, three dies from the center, middle, and edge of the package wafer are analyzed to examine the die location effect during wafer bending. At the RDL local scale, wafer bending and layout pattern effects on RDL reliability are examined. Between the scales, TCAD sub-modeling with buffer region technique is employed to extract upper scale solution as boundary constrains for lower scale analyses. The study also considers material effects with temperature dependent material properties and plastic deformation during thermal cycles.

10.6
Silicide based low temperature and low pressure bonding of Ti/Si for microfluidics and hermetic-sealing applications, C.Hemanth Kumar, Asisa Kumar Pnaigrahi*, Satish Bonam, Nirupam Paul, Siva Rama Krishna Vanjari, Shiv Govind Singh, Department of Electrical Engineering,Indian Institute of Technology Hyderabad,*Department of Electronics & Communication Engineering,Koneru Lakshmaiah Education Foundation- Hyderabad.

In this work, we have shown and validated bonding of titanium (Ti) coated glass with (100) silicon wafer at lower thermocompression cycle of 377 ˚C temperature and a nominal contact pressure of 0.15 MPa. Excellent bond strength > 100MPa and void free interface have been observed using scanning acoustic tomography (SAT), which clearly suggest that optimized temperature-pressure together can provide a superior quality bonding. Furthermore, post-bond dicing was performed in order to validate further the bonding strength which was confirmed by successfully dicing the Glass-Silicon pair without any damage to the bonding interface. This noble, low cost and low temperature simple bonding approach must be useful in hermetic sealing of microfluidic channels for on-chip compatible applications

10.7
A Highly Reliable 1x5um Via-last TSV Module, Stefaan Van Huylenbroeck, Yunlong Li, Joeri De Vos, Geraldine Jamieson, Nina Tutunjyan, Andy Miller, Gerald Beyer, Eric Beyne, imec

A 1x5um via-last TSV module is presented, coping with the reliability challenges imposed when exposing the metal landing pad during the liner opening etch at the TSV bottom. Two approaches are presented. A dedicated soft-landing liner oxide dry etch step is developed, eliminating the re-sputtering of copper on the TSV sidewalls. An embedded barrier is integrated, blocking the diffusion of any eventually re-sputtered copper of the landing pad. The obtained via-last TSV reliability is high for both approaches.

10.8
Strategy of Insertion of Merge Features in a Sea of Wires SADP Integration, J. H.-C. Chen, T. A. Spooner, L. A. Clevenger, M. O'Toole*, A. Ogino*, L. Lanzerotti*, S. Reidy*, C. Child*, IBM, *GLOBALFOUNDRIES

In BEOL, not only the minimum features, but wide lines are also important for power distribution. However, in the conventional SADP integration, insertion of wide features in the sea-of-wires area cannot be achieved easily. In this paper, five process schemes for insertion of complicate shapes were presented in this paper. These processes are designated as add on modules to boost the performance of the conventional SADP integration.

10.9

A Study on SADP Process Refresh for Patterning Correction, J. H.-C. Chen, I. C. Estrada, C. B. Peethala, Y. Mignot, H. Shobha, T. E. Standaert, IBM

In SADP integration, an accurate CD and profile control of mandrel patterning is important and an incorrect mandrel CD or profile could cause a huge loss. In this paper, a novel methodology suitable for high volume manufacturing is presented to remove the incorrect patterning stack and to refresh the SADP patterning from the beginning. As a result, the misprocessed wafer could continue the process without loss. Similar approaches could also be applied to FIN module.

10.10

Impact of Sn content in Ge1-xSnx layers on Ni stanogermanides solid-state reaction and properties, A. Quintero* **, P. Gergaud*, N. Chevalier*, J. Aubin*, J. M. Hartmann*, V. Loup*, V. Reboud*, E. Cassan** and Ph. Rodriguez*, * CEA LETI, ** CNRS, C2N

A comprehensive analysis focused on the impact of Sn content in GeSn layers, on Ni-based contacts, is presented. In-situ XRD, AFM and Rsh measurements were performed in order to follow phase growth, surface morphological evolution and electrical properties as the annealing temperature changed. Potential impact of those evolutions on devices integration is also discussed.

10.11

Effective Methods Controlling Cu Overburdens for Cu RDL Process, K. Park, J. Lee, B Yoo, Hanyang University

Microcontact printing (μCP) and electrochemical polishing (ECP) were proceeded for the Cu overburden thickness reduction and Cu planarization during the redistribution layer process. The suppressing property of μCP and the polishing effect of ECP were confirmed by electrochemical analysis. Suppressing effect of top surface of trench was confirmed after the μCP and Cu filling, and the removal of Cu overburdens was also confirmed after the Cu filling and the ECP.

10.12

Physical and Electrical Properties of New Zr Precursors with High Thermal Stability for High-k, H. D. Lim, S. Y. Jeon, W. M. Chae, J. J. Park, S. J. Yim, S. I. Lee, M. W. Kim, DNF Corporation

New Zr precursors have been developed using a tri-amine structure with enhanced thermal stability. The ALD window of the tri-amine structure is 220 to 320 degrees Celsius. In the capacitor structure with aspect ratio of 60 to 1, the step coverage was 99 percent. The dielectric constants of the ZrO2 thin films using tri-amine structure were improved by up to 13 percent and the leakage currents were similar to those of the cyclopentadienyl structure.

10.13

Oxidation Structure Change of Copper Surface Depending on Accelerated Humidity, P. Gomasang, S. Ogiue, K. Ueno, S. Yokogawa*, Shibaura Institute of Technology, *The University of Electro-Communication

For long-term reliability of Cu film in an environment, humidity dependence of the sheet resistance increase has been studied. We observed that resistance increase at 85% RH was almost the same to that of 75% RH in spite of higher oxidation. The nonlinear phenomena can be explained by the difference in the Cu oxide structure. The results suggest that lower humidity acceleration will be more appropriate in the THS test for passivated Cu to estimate the moisture resistance life because the real usage is typically in lower humidity.

10.14

Non-Reagent Express Metrology for Modern Damascene Copper Plating Baths, Michael Pavlov, Danni Lin, ECI Technology

The capability of analyzing all components in modern copper electroplating baths using non-reagent methods is demonstrated. The concentration of copper in new plating baths is significantly lower than in traditional baths. This article presents the results of our most recent study of the behavior of organic additives at low copper concentrations. The analytical results of our new methods for all bath components are presented.

10.15

Stress induced densification of thin porous low-k films during nanoindentation, O. O. Okudur*, M. Redzheb**, K. Vanstreels**, H. Zahednamesh**, M. Gonzalez**, I. De Wolf*, *KU Leuven and imec, **imec

Simultaneous impact of the substrate and pore densification hinders their differentiation during nanoindentation of porous thin low-k films, causing significant loss of valuable information in terms of nonlinear mechanical behavior. In this paper, we propose a method to overcome this issue by utilizing three nanoindenter probes that generate substantially different stress levels and elastic field distributions. The experimental results are benchmarked with FE simulations using Gurson model for porous media. The proposed multiple-probe approach could facilitate non-linear property characterization of fabricated low-k materials.

10.16

Integration of Metallization Processes in Robust Interconnects Formation for 14 nm Nodes and beyond, Nicolai Petrov, Shao Beng Law, Jonathan Rullan, Seungman Choi, San Leong Liew, Han Wah Ng, Shinichiro Kakita, GLOBALFOUNDRIES

In this communication the results of metallization processes integration to create robust Cu interconnects for advanced 14 nm and beyond nodes are presented. Conventional Dual Damascene BEOL process flow to form 64 nm pitch on-chip Cu interconnects in low-k dielectric substrate was utilized. TaN/Ta/Cu seed were formed by PVD, Cu lines were fabricated by Cu ECP followed by CMP.

10.17

Electrolytic Cobalt Fill of Sub-5 nm Node Interconnect Features, F. Wafula, J. Wu, S. Branagan, H. Suzuki, A. Gracias, J. van Eisden, Atotech USA LLC.

Electrolytic cobalt fill of sub-5 nm node features and a proposed model for the fill mechanism supported by cyclic voltammetry is presented. The transformation of the organic plating additive from an active to a de-activated state at the bottom of the feature is suggested as the mechanism of cobalt bottom-up fill. Plating results in features with 2- and – 4 nm pre-plate openings show void-free fill.

10.18

An Innovative System Integration Interconnection Technology Beyond BEOL, Dyi-Chung Hu, SiPlus Co.

The goal of this study is to verify an innovative system integration technology that integrates the connections beyond the I/Os of the chips. As the signals come out from the IC chip, it passes through UBM, bumps and solders in order to connect to the outside world. But the line density of the substrate underneath the die can’t shrink as fast as the Moore’s law. Hence the packaging industry developed the interposer (2.5D) on top of the substrate to solve the fine line requirement of substrate. The advanced chip packaging structure includes components of interposer, substrate and PCB. Each connection component needs a core to support during manufacturing process. The final packaging structure uses solders to connect between

interposer, substrate and PCB. The solders are left in the final packaging structure. In this paper, a new structure that do not need the cores and most of solders in the final packaging structure is proposed and tested. This new system integration packaging structure is a solder-minimum, TSV-less and core-less structure. A test chip with 10,000 bumps and 50µm pitch has been designed and manufactured to test this new structure. This new substrate structure composed of two portions; thin film fine line and laminated dielectric. The dimensional changes of the new test substrate were under control to be less than 4µm in 10mm range. Further bonding of the test chips to the new substrate was verified using a commercial TCB bonder.

10.19
Gas Phase Pore Stuffing (GPPS), M. Fujikawa, T. Yamaguchi, S. Nozawa, R. Niino, R. Chanson*, K. Babaei Gavan*, F. Lazzarino*, J-F. de Marneffe*, Tokyo Electoron Technology Solutions Limited, *Imec v.z.w.

Porous low-k dielectrics play an important role in lowering the circuit capacitance in nano-interconnects. However, these materials are damaged during plasma etching process and subsequent steps, leading to a degradation of their dielectric properties. We suggest a new method to solve the issue, so-called Gas Phase Pore Stuffing (GPPS). GPPS can fill the pores with sacrificail polymers by a single-step CVD process, and remove polymer by only Annealing.

10.20
Cu Barrier Properties of Cluster-Preforming-Deposited Amorphous WSin Films Depending on Composition n, N. Okada, N. Uchida, S. Ogawa, T. Kanayama, AIST

The thin amorphous WSin film with n =12 exhibited excellent diffusion barrier properties for Cu: an estimated TDDB lifetime > 10 years at 100 °C under 5 MV/cm stress for Cu MOS capacitors and a high barrier stability against annealing up to 600 °C for Cu on Si diodes. In addition, in the WSin (n =5−12) film in contact with Cu, the Si atoms do not diffuse into the Cu layer in spite of the Si-rich composition even at 300 °C. When n is 12, the WSin film has the most excellent thermal stability. From the ab-initio simulations, these properties are attributed to the fact that in the film, all the Si atoms are strongly bonded to the negatively charged W atoms. These results indicate that the WSi12 film is a promising barrier film against Cu.

10.21
Charge-Trap-Free Polymer-Liner Through-Silicon Vias for Reliability Improvement of 3D ICs, H. Kino, S. Lee, Y. Sugawara, T. Fukushima, T. Tanaka, Tohoku University

In this study, MIS capacitors with blind TSV structures using PI, BCB or PBO liners were fabricated and evaluated. In the case of BCB and PBO liners, remarkable hysteresis suppressions of the C-V curves was observed as compared to that of the PI liner. These results indicate that polar character is one of the most important characters for suppression of the capacitance modulation around TSVs and the detrapped-charge-induced signal noise.

10.22
Spray Plasma Processing of Barrier Films Deposited in Air for Improved Stability of Flexible Electronic Devices, Nicholas Rolston[1], Adam D. Printz[1], Florian Hilt[1], Michael Q. Hovish[1], Karsten Brüning[2], Christopher J. Tassone[2], Reinhold H. Dauskardt[1], [1]Stanford University, [2]SSRL, SLAC National Accelerator Laboratory

We report on submicron organosilicate barrier films produced rapidly in ambient by a scalable spray plasma process for improved solar cell stability. The plasma is at a sufficiently low temperature to be compatible with flexible electronic devices. The morphology and density of the barrier are shown to improve with the

addition of a fluorine-based precursor. Thin-film perovskite solar cells with submicron coatings exhibited significant improvements in stability when exposed to light, heat, and moisture.

10.23
Advanced metallization processes integration as manufacturing worthy solutions for >10:1 aspect ratio mid-process TSV, Thierry Mourier, Mathilde Gottardi, Céline Ribière, Gilles Romero*, Stéphane Minoret, Pierre-Emile Philip*, CEA Leti, *STMicroelectronics

This paper presents the evaluation of alternative metallization solutions able to overcome the actual limitations of TSV form factor and enable >10:1 aspect ratio mid-process TSV. Process choices and development are described and electrical results of the integration of these materials and processes are presented showing excellent yield, performances and distribution

6:30 pm
End of Sessions

Thursday, June 7

Session 11 - Process Integration 3

Session Chairs: Toshiaki Hasegawa, Terry Spooner

8:15 AM 11-1
Interconnect Stack using Self-Aligned Quad and Double Patterning for 10nm High Volume Manufacturing (Invited), **A. Yeoh**, A. Madhavan, N. Kybert, S. Anand, J. Shin, M. Asoro, S. Samarajeewa, J. Steigerwald, C. Ganpule, M. Buehler, A. Tripathi, V. Souw, M. Haran, S. Nigam, V. Chikarmane, P. Yashar, T. Mulé, Y-H. Wu, K-S. Lee, M. Aykol, K. Marla, P. Sinha, S. Kirby, H. Hiramatsu, W. Han, M. Mori, M. Sharma, H. Jeedigunta, M. Sprinkle, C. Pelto, M. Tanniru, G. Leatherman†, K. Fischer, I. Post, C. Auth, Intel Corporation

This paper describes Intel's 10nm high performance logic technology interconnect stack featuring 13 metal layers comprising two self-aligned quad patterned and four self-aligned double patterned layers. Quad patterned interconnect layers are introduced to continue Moore's Law, i.e. sub-40nm interconnect pitches to enable 10nm node cells that include 34nm fin pitch and Contact-over-active-gate (COAG) layout. Cobalt metallization is introduced in the pitch quartered interconnect layers in order to meet electromigration and gapfill-resistance requirements.

8:45 AM 11-2
Process Challenges in Fully Aligned Via Integration for sub 32 nm Pitch BEOL (Invited), **Benjamin D. Briggs**, C. B. Peethala, D. L. Rath, J. Lee, S. Nguyen, N. V. LiCausi*, P. S. McLaughlin, H. You*, D. Sil, N. A. Lanzillo, H. Huang, R. Patlolla, T. Haigh Jr, Y. Xu, C. Park*, P. Kerber, H. K. Shobha, Y. Kim**, J. Demarest, J. Li, G. Lian, M. Ali, C. t Le, E. T. Ryan*, L. A. Clevenger, D. F. Canaperi, T. E. Standaert, G. Bonilla, and E. Huang, IBM; *GLOBALFOUNDRIES Inc.; **Samsung Electronics

As BEOL pitch continues to aggressively scale, contributions from pattern dimension and edge placement constrict the available geometry of interconnects. In particular, the critical minimum insulator spacing which defines a technologies max operating voltage is now limited by Vx to Mx spacing. This spacing has historically been a challenge since the introduction of self-aligned vias due to the loss of CD and chamfer control in the non-self-aligned direction. As pitch continued to shrink from self-aligned via introduction around the 22 nm node, the fraction of via CD control and edge placement compared to the dielectric spacing between interconnects has continued to grow. Alone this trend could be combated by increasing

the dielectric spacing, however, the exponential increase in Cu resistivity (under scaling) has forced BEOL technologies into strong line/space asymmetry to keep line resistance under control. At pitches below 32 nm these factors reach a tipping point, either design to exponentially increasing line resistance or lower the technology Vmax. Both approaches cause performance degradation to achieve pitch scaling

9:15 AM 11-3
PVD-Treated ALD TaN for Cu Interconnect Extension to 5nm Node and Beyond, Z. Wu, R. Li, X. Xie, W. Suen, J. Tseng, N. Bekiaris, R. Vinnakota, K. Kashefizadeh, M. Naik, Applied Materials, Inc.

We report a novel approach to enable thin (≤15Å) ALD-based TaN barriers. The use of a post-ALD treatment in a PVD chamber resulted in ALD films with resistivity, density and Ta/N ratio similar to industry-standard PVD TaN. This approach enables conformal Cu barrier without reliability degradation compared to PVD TaN. This new approach overcomes the shadowing effect of the traditional PVD approach, improves the metal-fill process window, and promotes lower via resistance through barrier thickness reduction, proving it to be a viable Cu-barrier candidate for 5nm node and beyond.

9:40 AM 11-4
Interconnect Challenges and Opportunities in the Memory Space (Invited),
John Smythe, Marko Milojevic, Greg Herdt, Sumeet Pandey, Richard Hill, Micron Technology, Inc.

Interconnect requirements of logic and memory share the same categories of mechanical, metallurgical and electrical principles. The details of thermal budget, on-pitch features and aspect ratio have motivated an increase in the number of different approaches. Specific cases will be reviewed that span chemistry, materials, methods and related topics to support the nature of unique challenges within the scope of memory technology scaling.

10:10 am
BREAK

Session 12 - Materials and Unit Process 2 - Metals

Session Chairs: Vimal Manineni, Zsolt Tokei

10:30 AM 12-1
Alternative Metals: from ab initio Screening to Calibrated Narrow Line Models (Invited),
Christoph Adelmann, Kiroubanand Sankaran, Shibesh Dutta*, Anshul Gupta, Shreya Kundu, Geraldine Jamieson, Kristof Moors**, Nicolò Pinna, Ivan Ciofi, Sven Van Elshocht, Jürgen Bömmels, Guillaume Boccardi, Christopher J. Wilson, Geoffrey Pourtois,*** and Zsolt Tőkei, Imec; *KU Leuven, **University of Luxembourg, ***University of Antwerp

We discuss the selection and assessment of alternative metals by a combination of ab initio computation of electronic properties, experimental resistivity assessments, and calibrated line resistance models. Pt-group metals as well as Nb are identified as the most promising elements, with Ru showing the best combination of material properties and process maturity. An experimental assessment of the resistivity of Ru, Ir, and Co lines down to ~30 nm2 is then used to devise compact models for line and via resistance that can be compared to Cu predictions. The main advantage of alternative metals originates from the possibility for barrierless metallization.

11:00 AM 12-2
Metals for low-resistivity interconnects, Daniel Gall

A combination of experiments and first-principles simulations are used to search for metals that have a high conductivity at reduced dimensions and are therefore promising candidates for narrow interconnect lines. Epitaxial layers of Cu, W, Ta, Mo, Ru, Co, Ag, Nb and Ni are grown on ceramic single crystal substrates and their resistivity measured in-situ as a function of thickness. The measured values are directly compared to predictions using first-principles calculations of the most conductive elements.

11:25 AM 12-3
Metallic ceramics for low resitivity interconnects: an ab initio insight, K. Sankaran, K. Moors*, S. Dutta, C. Adelmann, Z. Tőkei, G. Pourtois**, IMEC, *University of Luxembourg, **University of Antwerp

The scalability potential of low resistivity ternary metallic alloys (MAX) as an interconnect medium has been benchmarked against copper through first-principle simulations.

11:50 PM 12-4
A First-Principles Density Functional Theory based framework for barrier material screening, G. Hegde, R. C. Bowen, H. Simka, Advanced Logic Lab, Samsung Semiconductor Inc (SSI)

A first principles Density Functional Theory (DFT) based framework for barrier material screening is described. The vertical component of barrier resistance - a crucial component of via resistance difficult to access through experiments - is estimated by statistically averaging electron transmission from an ensemble of transport calculations in the Non-Equilibrium Greens Function (NEGF) formalism. The framework is successfully validated for the TaxNy system using datasets in the literature. Use of the framework as a first step towards predictive barrier material screening is illustrated, by comparing TaxNy with a different class of material.

12:15 pm
LUNCH

Session 13 - Materials and Unit Process 3 - Metals

Session Chairs: Luke Henderson, Romy Liske

1:30 PM 13-1
Resistance Scaling of Cu Interconnect and Alternate Metal (Co, Ru) Benchmark toward sub 10nm Dimension, He Ren, Zhiyuan Wu, Nikos Bekiaris, Jennifer Tseng, Gary How, Xiangjin Xie, Wei Lei, Rong Tao, Roey Shaviv, Joung Joo Lee, Ramkumar Vinnakota, Keyvan Kashefizadeh, Max Gage, Mehul Naik, Applied Materials, Inc.

Interconnect line resistance at smaller dimension is a critical scaling roadblock. While efforts continue to manage resistance of Cu interconnect, Cu replacements such as Co, Ru are under active consideration as next generation interconnects. It is important to characterize how these metals scale with respect to each other to provide input into the technology roadmap. Here, we present our work on resistance benchmarking of Cu, Co and Ru interconnects down to less than 10nm CD to help shed light from a scaling perspective.

1:55 PM 13-2
Embedded metal voids detection to improve Copper metallization for advanced interconnect, J. Tseng, Applied Materials, Inc

We present here our studies on using electron beams to locate copper fill voids in dual damascene structures down to 10nm CD. It is shown that the e-beam technique can be optimized for detecting embedded voids in non-destructive manner that enables faster process development on 300mm wafers by reducing the dependence on time consuming methods such as Transmission Electron Microscope (TEM), while at the same time providing statistically significant information during process development and monitoring.

2:20 PM 13-3
Damascene benchmark of Ru, Co and Cu in scaled dimensions, Marleen H. van der Veen, N. Heylen, O. Varela Pedreira, I. Ciofi, S. Decoster, V. Vega Gonzalez, N. Jourdan, H. Struyf, K. Croes, C. J. Wilson, Zs. Tőkei, Imec

The alternative metals Ru and Co are benchmarked to Cu in a damascene vehicle at scaled dimensions. Ru and Co are found to be superior in line resistance for trenches smaller than 250nm2. The work is complemented with a via R modelling and EM performance comparison. Here, the barrierless Ru is superior at both levels.

2:45 pm
BREAK

Session 14 - 3D Process and Integration

Session Chairs: Valeriy Sukharev, Tetsu Tanaka

3:05 PM 14-1
From direct bonding mechanism to 3D applications (Invited),
F. Fournel, H. Moriceau, V. Larrey,C. Morales, C. Mauguen, C. Bridoux
Univ. Grenoble Alpes, CEA, LETI

Nowadays Silicon direct wafer bonding is a mass production technology in many different applications. Starting around the sixties for industrial optical system elaboration, its major development is now in the microelectronic, microtechnology and optoelectronic fields. Obviously to reach such a mature level, the direct bonding mechanisms have to be established. The silicon or silicon dioxide direct bonding is now well established and direct bonding using metallic surfaces starts also to be investigated. For instance, copper or titanium direct bonding mechanism are established. The behavior of hybrid direct bonding using surfaces composed of both materials can then be understood. This hybrid bonding paves the way to high-density interconnection bonding for 3D applications.

3:35 PM 14-2
Advances in SiCN-SiCN Bonding with High Accuracy Wafer-to-Wafer (W2W) Stacking Technology, L. Peng, S-W Kim, S. Iacovo, F. Inoue, A. Phommahaxay, E. Sleeckx, J. De Vos, D. Zinner*, T. Wagenleitner*, T. Uhrmann*, M. Wimplinger*, B. Schoenaers**, A. Stesmans**, V. V. Afanas'ev**, A. Miller1, G. Beyer1, E. Beyne1, IMEC, *EV Group, **University of Leuven

Results are presented of recent studies in material exploration for W2W bonding and advanced W2W alignment carried out as a holistic approach to enable a robust ultra-fine pitch interconnect for 3Dsystem-on-chip (SoC) technology.

4:00 PM 14-3

Novel Bonding Process Using Ultra-thin Mn for Highly Robust and Reliable Cu/SiO Hybrid Bonding, K. Uchida, K. Tsumura, K. Nakamura, K. Higashi, Y. Sugizaki, H. Shibata, Toshiba Corporation

We suggest a new Cu/SiO hybrid bonding process using ultra-thin Mn film at the bonding interface. In this process, bonding stability can be improved because bonding interface consists of only Mn. In addition,Mn on SiO forms MnSiO dielectric known as diffusion barrier for Cu during thermal process, results in improving the reliability of interconnects at misalignment area. In order to prove the possibility of this process, we evaluated bonding strength of Mn/Mn interface and electric property of oxidized Mn film. Good bonding strength was obtained at the condition of annealing at 350°C or more temperature. Moreover, it was confirmed that the resistivity of ultra-thin Mn film on SiO layer was increased by heat treatment.

4:25 PM 14-4

3D packaging+Cooling --- "Beat the heat in 3D Chip stacks with Novel microfluidics" (Invited), T. Chainer, **P. R. Parida**, M. Schultz, F. Yang, M. Gaynes, G. McVicker, A. Sridhar, S. Paredes, O. Ozsun, T. Brunschwiler, U. Drechsler, E. Colgan, B. Dang, Y. Liu, Q. Chen, A. Buyuktosunoglu, A. Vega, Y. Kwark, L. Shan, D. Liu, J. Silbermann, B. Webb, R. Joshi, J. Knickerbocker, C. Tyberg
IBM

In the Moore's Law race to keep improving computer performance, the IT industry has turned upward, stacking chips into skyscrapers. The 3D chip stacking technology has the potential to enable increased system performance through close integration of heterogeneous system components such as accelerators and/or high-density memory. However, 3D chips stacks, like the law they are challenging, have limits due to heat generation. A solution to remove the heat in 3D stacks is embedded cooling in which a benign nonconductive dielectric fluid (like the one used in refrigeration systems) is made to flow through microscopic gaps, some no wider than a single strand of hair (~100 μm), between the stacked high power active layers [1-2]. This dielectric fluid can come into contact with electrical connections, so is not limited to one part of a chip or stack. The fluid is pumped into the chips, where it removes the heat from the chip by boiling from liquid-phase to vapor-phase. The vapor is then condensed back to liquid and recirculated. This two-phase cooling technology not only delivers a lower device junction temperature (Tj), but also reduces system size, weight, and power consumption [3-5].

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