Wednesday, June 6

Session 10

4:40 pm - Poster Session and Reception

10.1

Tungsten Plug Missing Defects Monitoring Method and Its Solution by Optimization of Polymer Cleaning and Micro-environment, Rongwei Fan*, Hunglin Chen, Kai Wang, Yin Long, Qiliang Ni,Shanghai Huali Microelectronics Corporation

This paper describes the tungsten (W) missing defects monitoring method with electron-beam inspection systems, and its solution by optimization of polymer cleaning and micro-environment. W missing defects detection and monitoring method was developed and fixed on bare silicon wafer. Then a series of experiments was carried out, and W missing defects were fixed by the optimization of polymer cleaning and micro-environment of the front side open unit port (FOUP).

10.2

Silicon Trench Etch Uniformity Improvement for Microloading and Macro-to-Macro Loading for sub-14nm Node, Y. Yang, S. Lim, J. Hong, M. Park, Y. Yang, W. Cho, C. Adams, M. Aminpur, and C. Maeng, GLOBALFOUNDRIES

We report a test and demonstration of plasma etching conditions that can be applied in advanced nodes beyond 14nm patterning to relieve trench depth sensitivity to incoming CD variations caused by multipatterning and macro-to-macro loading impacts from pattern density. Our result showed that lower RF duty cycle, higher bias voltage, and higher etchant flow can reduce 50% of the depth variation to incoming CD variations caused by multipatterning in previous steps and 75% of the depth differences between dense and isolated pattern areas for macro-to-macro loading.

10.3

Modulation of Within-wafer and Within-die Topography for Damascene Copper in Advanced Technology, W.-T. Tseng, T.-J. Cheng, S. Ahmed, J. Lee, F. Baumann, GLOBALFOUNDRIES

A novel copper electroplating and CMP process was developed to effectively modulate the within-wafer and within-die nanoscale topography. The feasibility of this new metallization is demonstrated on a 64nm pitch product with an equivalent defect level, lower and tighter distribution in resistance and trench height. It's believed to be extendable to other advanced nodes for a sizable reduction in copper overburden which saves CMP polish cycle time from the plan-of-record time.

10.4

The impact of solute segregation on grain boundaries in dilute Cu alloys, Takanori Tsurumaru, Luke Prestowitz*, Brendan O'Brien* and Kathleen Dunn*, SUMCO Corporation/State University of New York Polytechnic Institute, *State University of New York Polytechnic Institute

Alloying copper with cobalt may offer a means for stabilizing grain boundaries against electromigration void formation in advanced interconnects. Here we present a means for co-depositing dilute copper alloys, using Co and Ag as the solutes of interest. Microstructure and compositional analysis are presented.

10.5
Modeling wafer bending effects on RDL layer reliability in a multiple die package, Tzu Chen Wang, Chih Chieh Yeh, Xiaopeng Xu, Karim El Sayed, Chun-Hung Steven Lin*, Synopsys Inc., *Corning Display Technologies

Wafer bending effects on re-distribution layer (RDL) reliability in a multiple die package is examined using multiscale TCAD sub-modeling techniques. At the global scale, the wafer package with 200 dies and 3 RDL layers is analyzed with smear material representation. At the die scale, three dies from the center, middle, and edge of the package wafer are analyzed to examine the die location effect during wafer bending. At the RDL local scale, wafer bending and layout pattern effects on RDL reliability are examined. Between the scales, TCAD sub-modeling with buffer region technique is employed to extract upper scale solution as boundary constrains for lower scale analyses. The study also considers material effects with temperature dependent material properties and plastic deformation during thermal cycles.

10.6
Silicide based low temperature and low pressure bonding of Ti/Si for microfluidics and hermetic-sealing applications, C.Hemanth Kumar, Asisa Kumar Pnaigrahi*, Satish Bonam, Nirupam Paul, Siva Rama Krishna Vanjari, Shiv Govind Singh, Department of Electrical Engineering,Indian Institute of Technology Hyderabad,*Department of Electronics & Communication Engineering,Koneru Lakshmaiah Education Foundation- Hyderabad.

In this work, we have shown and validated bonding of titanium (Ti) coated glass with (100) silicon wafer at lower thermocompression cycle of 377 ˚C temperature and a nominal contact pressure of 0.15 MPa. Excellent bond strength > 100MPa and void free interface have been observed using scanning acoustic tomography (SAT), which clearly suggest that optimized temperature-pressure together can provide a superior quality bonding. Furthermore, post-bond dicing was performed in order to validate further the bonding strength which was confirmed by successfully dicing the Glass-Silicon pair without any damage to the bonding interface. This noble, low cost and low temperature simple bonding approach must be useful in hermetic sealing of microfluidic channels for on-chip compatible applications

10.7
A Highly Reliable 1x5um Via-last TSV Module, Stefaan Van Huylenbroeck, Yunlong Li, Joeri De Vos, Geraldine Jamieson, Nina Tutunjyan, Andy Miller, Gerald Beyer, Eric Beyne, imec

A 1x5um via-last TSV module is presented, coping with the reliability challenges imposed when exposing the metal landing pad during the liner opening etch at the TSV bottom. Two approaches are presented. A dedicated soft-landing liner oxide dry etch step is developed, eliminating the re-sputtering of copper on the TSV sidewalls. An embedded barrier is integrated, blocking the diffusion of any eventually re-sputtered copper of the landing pad. The obtained via-last TSV reliability is high for both approaches.

10.8
Strategy of Insertion of Merge Features in a Sea of Wires SADP Integration, J. H.-C. Chen, T. A. Spooner, L. A. Clevenger, M. O'Toole*, A. Ogino*, L. Lanzerotti*, S. Reidy*, C. Child*, IBM, *GLOBALFOUNDRIES

In BEOL, not only the minimum features, but wide lines are also important for power distribution. However, in the conventional SADP integration, insertion of wide features in the sea-of-wires area cannot be achieved easily. In this paper, five process schemes for insertion of complicate shapes were presented in this paper. These processes are designated as add on modules to boost the performance of the conventional SADP integration.

10.9

A Study on SADP Process Refresh for Patterning Correction, J. H.-C. Chen, I. C. Estrada, C. B. Peethala, Y. Mignot, H. Shobha, T. E. Standaert, IBM

In SADP integration, an accurate CD and profile control of mandrel patterning is important and an incorrect mandrel CD or profile could cause a huge loss. In this paper, a novel methodology suitable for high volume manufacturing is presented to remove the incorrect patterning stack and to refresh the SADP patterning from the beginning. As a result, the misprocessed wafer could continue the process without loss. Similar approaches could also be applied to FIN module.

10.10

Impact of Sn content in Ge1-xSnx layers on Ni stanogermanides solid-state reaction and properties, A. Quintero* **, P. Gergaud*, N. Chevalier*, J. Aubin*, J. M. Hartmann*, V. Loup*, V. Reboud*, E. Cassan** and Ph. Rodriguez*, * CEA LETI, ** CNRS, C2N

A comprehensive analysis focused on the impact of Sn content in GeSn layers, on Ni-based contacts, is presented. In-situ XRD, AFM and Rsh measurements were performed in order to follow phase growth, surface morphological evolution and electrical properties as the annealing temperature changed. Potential impact of those evolutions on devices integration is also discussed.

10.11

Effective Methods Controlling Cu Overburdens for Cu RDL Process, K. Park, J. Lee, B Yoo, Hanyang University

Microcontact printing (μCP) and electrochemical polishing (ECP) were proceeded for the Cu overburden thickness reduction and Cu planarization during the redistribution layer process. The suppressing property of μCP and the polishing effect of ECP were confirmed by electrochemical analysis. Suppressing effect of top surface of trench was confirmed after the μCP and Cu filling, and the removal of Cu overburdens was also confirmed after the Cu filling and the ECP.

10.12

Physical and Electrical Properties of New Zr Precursors with High Thermal Stability for High-k, H. D. Lim, S. Y. Jeon, W. M. Chae, J. J. Park, S. J. Yim, S. I. Lee, M. W. Kim, DNF Corporation

New Zr precursors have been developed using a tri-amine structure with enhanced thermal stability. The ALD window of the tri-amine structure is 220 to 320 degrees Celsius. In the capacitor structure with aspect ratio of 60 to 1, the step coverage was 99 percent. The dielectric constants of the ZrO2 thin films using tri-amine structure were improved by up to 13 percent and the leakage currents were similar to those of the cyclopentadienyl structure.

10.13

Oxidation Structure Change of Copper Surface Depending on Accelerated Humidity, P. Gomasang, S. Ogiue, K. Ueno, S. Yokogawa*, Shibaura Institute of Technology, *The University of Electro-Communication

For long-term reliability of Cu film in an environment, humidity dependence of the sheet resistance increase has been studied. We observed that resistance increase at 85% RH was almost the same to that of 75% RH in spite of higher oxidation. The nonlinear phenomena can be explained by the difference in the Cu oxide structure. The results suggest that lower humidity acceleration will be more appropriate in the THS test for passivated Cu to estimate the moisture resistance life because the real usage is typically in lower humidity.

10.14
Non-Reagent Express Metrology for Modern Damascene Copper Plating Baths, Michael Pavlov, Danni Lin, ECI Technology

The capability of analyzing all components in modern copper electroplating baths using non-reagent methods is demonstrated. The concentration of copper in new plating baths is significantly lower than in traditional baths. This article presents the results of our most recent study of the behavior of organic additives at low copper concentrations. The analytical results of our new methods for all bath components are presented.

10.15
Stress induced densification of thin porous low-k films during nanoindentation, O. O. Okudur*, M. Redzheb**, K. Vanstreels**, H. Zahednamesh**, M. Gonzalez**, I. De Wolf*, *KU Leuven and imec, **imec

Simultaneous impact of the substrate and pore densification hinders their differentiation during nanoindentation of porous thin low-k films, causing significant loss of valuable information in terms of nonlinear mechanical behavior. In this paper, we propose a method to overcome this issue by utilizing three nanoindenter probes that generate substantially different stress levels and elastic field distributions. The experimental results are benchmarked with FE simulations using Gurson model for porous media. The proposed multiple-probe approach could facilitate non-linear property characterization of fabricated low-k materials.

10.16
Integration of Metallization Processes in Robust Interconnects Formation for 14 nm Nodes and beyond, Nicolai Petrov, Shao Beng Law, Jonathan Rullan, Seungman Choi, San Leong Liew, Han Wah Ng, Shinichiro Kakita, GLOBALFOUNDRIES

In this communication the results of metallization processes integration to create robust Cu interconnects for advanced 14 nm and beyond nodes are presented. Conventional Dual Damascene BEOL process flow to form 64 nm pitch on-chip Cu interconnects in low-k dielectric substrate was utilized. TaN/Ta/Cu seed were formed by PVD, Cu lines were fabricated by Cu ECP followed by CMP.

10.17
Electrolytic Cobalt Fill of Sub-5 nm Node Interconnect Features, F. Wafula, J. Wu, S. Branagan, H. Suzuki, A. Gracias, J. van Eisden, Atotech USA LLC.

Electrolytic cobalt fill of sub-5 nm node features and a proposed model for the fill mechanism supported by cyclic voltammetry is presented. The transformation of the organic plating additive from an active to a de-activated state at the bottom of the feature is suggested as the mechanism of cobalt bottom-up fill. Plating results in features with 2- and – 4 nm pre-plate openings show void-free fill.

10.18
An Innovative System Integration Interconnection Technology Beyond BEOL, Dyi-Chung Hu, SiPlus Co.

The goal of this study is to verify an innovative system integration technology that integrates the connections beyond the I/Os of the chips. As the signals come out from the IC chip, it passes through UBM, bumps and solders in order to connect to the outside world. But the line density of the substrate underneath the die can't shrink as fast as the Moore's law. Hence the packaging industry developed the interposer (2.5D) on top of the substrate to solve the fine line requirement of substrate. The advanced chip packaging structure includes components of interposer, substrate and PCB. Each connection component needs a core to support during manufacturing process. The final packaging structure uses solders to connect between

interposer, substrate and PCB. The solders are left in the final packaging structure. In this paper, a new structure that do not need the cores and most of solders in the final packaging structure is proposed and tested. This new system integration packaging structure is a solder-minimum, TSV-less and core-less structure. A test chip with 10,000 bumps and 50µm pitch has been designed and manufactured to test this new structure. This new substrate structure composed of two portions; thin film fine line and laminated dielectric. The dimensional changes of the new test substrate were under control to be less than 4µm in 10mm range. Further bonding of the test chips to the new substrate was verified using a commercial TCB bonder.

10.19
Gas Phase Pore Stuffing (GPPS), M. Fujikawa, T. Yamaguchi, S. Nozawa, R. Niino, R. Chanson*, K. Babaei Gavan*, F. Lazzarino*, J-F. de Marneffe*, Tokyo Electoron Technology Solutions Limited, *Imec v.z.w.

Porous low-k dielectrics play an important role in lowering the circuit capacitance in nano-interconnects. However, these materials are damaged during plasma etching process and subsequent steps, leading to a degradation of their dielectric properties. We suggest a new method to solve the issue, so-called Gas Phase Pore Stuffing (GPPS). GPPS can fill the pores with sacrificail polymers by a single-step CVD process, and remove polymer by only Annealing.

10.20
Cu Barrier Properties of Cluster-Preforming-Deposited Amorphous WSin Films Depending on Composition n, N. Okada, N. Uchida, S. Ogawa, T. Kanayama, AIST

The thin amorphous WSin film with n =12 exhibited excellent diffusion barrier properties for Cu: an estimated TDDB lifetime > 10 years at 100 °C under 5 MV/cm stress for Cu MOS capacitors and a high barrier stability against annealing up to 600 °C for Cu on Si diodes. In addition, in the WSin (n =5−12) film in contact with Cu, the Si atoms do not diffuse into the Cu layer in spite of the Si-rich composition even at 300 °C. When n is 12, the WSin film has the most excellent thermal stability. From the ab-initio simulations, these properties are attributed to the fact that in the film, all the Si atoms are strongly bonded to the negatively charged W atoms. These results indicate that the WSi12 film is a promising barrier film against Cu.

10.21
Charge-Trap-Free Polymer-Liner Through-Silicon Vias for Reliability Improvement of 3D ICs, H. Kino, S. Lee, Y. Sugawara, T. Fukushima, T. Tanaka, Tohoku University

In this study, MIS capacitors with blind TSV structures using PI, BCB or PBO liners were fabricated and evaluated. In the case of BCB and PBO liners, remarkable hysteresis suppressions of the C-V curves was observed as compared to that of the PI liner. These results indicate that polar character is one of the most important characters for suppression of the capacitance modulation around TSVs and the detrapped-charge-induced signal noise.

10.22
Spray Plasma Processing of Barrier Films Deposited in Air for Improved Stability of Flexible Electronic Devices, Nicholas Rolston[1], Adam D. Printz[1], Florian Hilt[1], Michael Q. Hovish[1], Karsten Brüning[2], Christopher J. Tassone[2], Reinhold H. Dauskardt[1], [1]Stanford University, [2]SSRL, SLAC National Accelerator Laboratory

We report on submicron organosilicate barrier films produced rapidly in ambient by a scalable spray plasma process for improved solar cell stability. The plasma is at a sufficiently low temperature to be compatible with flexible electronic devices. The morphology and density of the barrier are shown to improve with the

addition of a fluorine-based precursor. Thin-film perovskite solar cells with submicron coatings exhibited significant improvements in stability when exposed to light, heat, and moisture.

10.23
Advanced metallization processes integration as manufacturing worthy solutions for >10:1 aspect ratio mid-process TSV, Thierry Mourier, Mathilde Gottardi, Céline Ribière, Gilles Romero*, Stéphane Minoret, Pierre-Emile Philip*, CEA Leti, *STMicroelectronics

This paper presents the evaluation of alternative metallization solutions able to overcome the actual limitations of TSV form factor and enable >10:1 aspect ratio mid-process TSV. Process choices and development are described and electrical results of the integration of these materials and processes are presented showing excellent yield, performances and distribution

6:30 pm
End of Sessions