Selective Processes: Challenges and Opportunities in Semiconductor Scaling

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IITC 2018 Selective Deposition Workshop
Contents

- Technology trends: challenges and approach in patterning
- Selective Deposition opportunities and challenges
- Summary
Technology trends
Technology trend

Vertical utilization is the key approach towards sub-10nm generation
Logic trend and challenges

Advanced patterning technology is the key to continuous scaling and transistor structure evolution.
Design trend and challenges

2D layout

1D layout

Grid challenge

Poly Gate Pitch (nm)

Metal Pitch (nm)

0 40 80 120 160 200

200 160 120 80 40 0

Breakthrough for Scaling
Single Exposure
SADP
SAQP
Pitch walk
roughness

Poly Gate Pitch (nm)

0 40 80 120 160 200

Line cut challenge

Grid + Cut/block ➜ 1D layout

SAQP : Self-Aligned Quadruple Exposure

SAQP : Self-Aligned Quadruple Exposure

SADP : Self-Aligned Double Patterning

Layout decomposition to 1D is a break through to scaling, but also creates new challenges
Patterning challenges and approach
Patterning challenges

Grid formation

Grid formation

Line cutting

Line cutting

Final Pattern

\[ EPE = f(CD\ \text{variation, Pattern}\ OL) \]

(EPE : Edge Placement Error)

- Mandrel, spacer, cuts
- Traditional sources of CD variation
- Roughness

- Previous Pattern
- Cuts to the grid
- Cuts to each other

**EPE is the fundamental challenge for advanced patterning technology**
EPE requirement

**Cut mask case**

![Diagram showing cut mask case with EPE calculation formula: \( \sqrt{+ (\text{PitchError}_{\text{grating}})^2 + (\text{CDU}_{\text{hole}})^2 + (\text{Overlay})^2} \)

**BEOL case**

![Graph showing EPE vs. half pitch for Device requirement and Process-induced requirements]

Continuous EPE improvement is needed along with scaling.
Typical EPE factors

CD variation

- Roughness (LER / LWR / CER)
- Pattern profile (leaning)
- Etch clogging
- Loading effect

Overlay

- Alignment of cut/block to grid
- Alignment of via to metal lines
- Alignment of holes at multiple LE

Numerous factors impact EPE and should be addressed
Patterning paradigm towards placement accuracy

The paradigm is expanding to self-alignment and bottom up approach
# Patterning challenges and approaches

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<th>Typical scheme</th>
<th>Challenge</th>
<th>Potential approach</th>
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<td>Grid formation</td>
<td>SADP, SAQP</td>
<td>LER, LWR, local CDU</td>
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<td></td>
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<tr>
<td></td>
<td>Spacing leaning</td>
<td></td>
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<tr>
<td></td>
<td>Cost</td>
<td></td>
</tr>
<tr>
<td>Cut / Block</td>
<td>LEx</td>
<td>CD, CDU, CER</td>
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<td>Alignment with grid (within layer)</td>
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<td></td>
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<td>Cost and complexity mitigation</td>
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<tr>
<td>Via formation</td>
<td>LEx</td>
<td>CD, CDU, CER</td>
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<tr>
<td></td>
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<td>Alignment with metal lines (inter layers)</td>
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<td>Cost and complexity mitigation</td>
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<td>Bottom up lithography</td>
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</table>
Process technology examples
Self-alignment through etch selectivity

Intended design

Conventional approach using L/S grid

Self-aligned approach with 3 grid colors

Self-alignment of cut/block is enabled by SAB, using etch selectivity

Etch selects mandrel

Etch selects fill material

A Core

B Spacer

C Fill material

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Placement margin improvement by SAB

Conventional

half pitch 12 | 12

etch

Lithography OL is restricted to be within 6nm (regardless of 193i or EUV)

SAB

half pitch 36 | 36

etch

Lithography OL limit will be covered within the margin

(pitch assumption: 24nm)

Placement margin of hard mask is 3 times relaxed
Flexibility of material selection for SAB

Potential material combinations

<table>
<thead>
<tr>
<th>Case #</th>
<th>Mandrel (A)</th>
<th>Spacer (B)</th>
<th>Fill (C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>a-Si</td>
<td>MeOx</td>
<td>SOG</td>
</tr>
<tr>
<td>2</td>
<td>SiN</td>
<td>Oxide</td>
<td>SOC</td>
</tr>
<tr>
<td>3</td>
<td>a-Si</td>
<td>Oxide</td>
<td>SOM</td>
</tr>
</tbody>
</table>

SAB demonstration (case 2)

Combination of non-metal materials

Various material combinations can be implemented
Combination of non-metal materials is demonstrated
Atomic level process approach
Evolution of the Self-aligned Technology: New integration and material Innovation

**Self-Aligned**
- **SAMP** (self-aligned multiple patterning)
- **SAB** (self-aligned block)
- **SAC** (self-aligned contact)

SAMP requires ALD, which can control deposition thickness at the nm scale.

SAB is enabled by taking advantage of different etch selectivity between different combinations (complex material combination).

ALD and ALE are indispensable to SAC, which is now dominant in MOL contact.

**Self-Directed**

Selecting Deposition

Younkin SPIE 2015

**Self-Limited**

**Atomic Layer Deposition**

Repeat cycle N times

Säynätjoki 8 May 2012, SPIE Newsroom. DOI 10.1117/2.1201204.004218

**Atomic Layer Etching**

Kim JES EDL 158, 12, 2011, D710-4 doi: 10.1149/2.061112jes
Atomic Layer Deposition (ALD) technology

Initial | 1st reactant | Purge | Oxidation | Purge

Self-limited reaction (0.2nm / cycle)

Film coverage comparison

Conventional (CVD) | ALD

18/8/13nm | 18/12/16nm | 18/17/18nm | 18/18/18nm

uniform coverage

saturated

Conformal deposition is enabled by self-limited reaction at atomic level

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ALE Technology (AlOx example)

1. Etchant Adsorption
2. Etchant Purge
3. Etching Products Desorption
4. Etching Products Purge

Anisotropic ALE by self-limiting half cycles

Min Microelectronic Eng. 110 (2013) 457–460
Thermal ALE

Reverse ALD $\rightarrow$ through ligand exchange

Multiple options of atomic layer approach

<table>
<thead>
<tr>
<th>Approach</th>
<th>Atomic layer (A)</th>
<th>Several layers (B)</th>
<th>Ion Modification (C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic diagram</td>
<td>Adsorption step</td>
<td>Activation step</td>
<td>FC film adsorption by FC plasma</td>
</tr>
<tr>
<td>Loading</td>
<td>Free</td>
<td>Controlled by step parameter</td>
<td></td>
</tr>
<tr>
<td>Polymer</td>
<td>No use</td>
<td>Thin polymer</td>
<td></td>
</tr>
<tr>
<td>Etched film</td>
<td>Si, Ge</td>
<td>SiO₂, SiN</td>
<td></td>
</tr>
<tr>
<td>Throughput</td>
<td>Slow</td>
<td>OK</td>
<td></td>
</tr>
<tr>
<td>Selectivity</td>
<td>Infinite</td>
<td>High</td>
<td></td>
</tr>
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</table>

Optimal approach can be selected by the requirement of material combination, selectivity and throughput.
"Quasi-ALE" technology

SiO$_2$ etch

Initial

**Adsorption**
(radical transportation)

Several layers of adsorption

**Activation**
(ion bombardment)

Ar

**Desorption**

(ALE : Atomic Layer Etch)

**Example : Self-Aligned Contact**

Mask

1. High SiN selectivity
2. Narrow slit etch

**Conventional**

**Quasi-ALE**


High selective etch is enabled by independent control of radical and ion flux.
Novel SiN etch technology

Ion Modification step

Modified layer formation by ion activation

Chemical Removal step

Modified layer removal by radical reaction

Example: SiN spacer etch

Initial

Conventional

Novel process

High selective etch is enabled by semi self-limiting reaction of SiN

Si loss: 0.0nm
SiO2 loss: 1.6nm
Excellent footing
Selective Deposition Toolbox/Opportunities

Wallace, AVS, 2015
Area Selective Deposition (ASD)

**Objectives**

Device fabrication requires due to scaling to make simple process scheme

**Requirements**

1. Difference in surface chemistries between growth and non growth areas
2. Deposition on either Dielectric or Metal on Dielectric or Metal
3. No deposition on undesired surfaces
4. Orthogonal film growth

<table>
<thead>
<tr>
<th>Advantages</th>
<th>Litho. / Etch / Depo</th>
<th>Selective deposition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Current Scheme</td>
<td>No litho. / Etch process needed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>No scaling limit</td>
</tr>
</tbody>
</table>

| Concerns   | Multiple processes Impact CPW | New technology required |

**Diagram**:

- Growth on A
- Growth on B
- Selectivity regime
- Cycle/time
- Thickness
- Dielectric
- Metal or Si
- Depo.
Approaches to Area Selective Deposition (ASD)

- **ASD by Inherent Selectivity**
  - Metal on metal
  - Epitaxy of Si

- **ASD by Ligand/precursor design**
  - Precursor inhibition or reactant inhibition

- **ASD by Surface deactivation or activation**
  - Passivation by Self-assembled monolayer (SAM)

- **ASD by Combination of deposition and etch**
  - Topographically selective
  - Selectivity enhancement by correction step

- **ASD by Inhibition during ALD**
  - (ABC or ABCD) process
Selective deposition by inherent material selectivity (Example Metal on metal)

Deposition of Ru is demonstrated to grow on W only
Selective Deposition by Ligand Design

- Tailor precursor chemistry for favorable reactions on desired surfaces
- Need to be explored
Selective Deposition by Via Selective Precursor adsorption

Selective ALD Fe$_2$O$_3$ only growth on Pt when using O2 as co-reactant $\rightarrow$ growth occurs only on the catalytic active surface

Selective Deposition by Area Deactivation or Activation

SAM is used to block HfO2 growth on undesired surface while grows on desired surface

ALD Pt grows on Pt but not on Al2O3 surface at low pressure


Requirement for SAM Layer

- Tail group determines surface functionalization
- Head group determines substrate reaction
- Van der Waals ensures formation of ordered SAM

SAM needs to be densely pack and reasonably long chain

Lee and Bent, Wiley-VCH Verlag (2012)

### Types of SAMs

<table>
<thead>
<tr>
<th>Type</th>
<th>Formula</th>
</tr>
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<tbody>
<tr>
<td>Thiols</td>
<td>R-SH</td>
</tr>
<tr>
<td>Silanes</td>
<td>R-SiCl₃</td>
</tr>
<tr>
<td>Alkenes</td>
<td>R-C=C</td>
</tr>
<tr>
<td>Alkanoic acids</td>
<td>R-CO₂H</td>
</tr>
<tr>
<td>Phosphonic acids</td>
<td>R-PO₃H₃</td>
</tr>
</tbody>
</table>


Densely packed long chain SAM

Densely packed short chain SAM

SAM with bulky tail groups

Loosely packed SAM with pinholes
Area selective deposition by combining Deposition and Etch: topographically selective

Note: Very high selectivity to SiO₂

ALD high K dielectrics followed by anisotropic ALE enables thin ALD sidewall spacers
Area selective deposition by combining ALD and etch: topographically selective

Woo-hee Kim et al., ACS Nano, 10, 4451 (2016)

Selective Pt thin film using topographically selective inhibition
Selective deposition via inhibition during deposition Dielectric on dielectric

Si substrate treatment:
- HDHD: Adding H radical treatment during after every x cycles to inhibit growth
  - Delayed ALD Al₂O₃ incubation
  - Super ALD cycles → [X (AB cycles)+H treatment]×Y

SPA H plasma is effective in suppressing Al₂O₃ growth up to ~5nm on Si and not on oxides

K. Tapily, AVS Focus Topic Selective Deposition, San Jose 2015
ASD using inhibition during ALD (ABC or ABCD) process

- Inhibitor selectively absorbed
- Inhibitor blocks growth
- Inhibitor is removed during co-reactant

Selectivity achieved via precursor deactivation using in situ inhibitor (Hacac)

Different selectivity observed for different oxide surfaces

Mameli et al., ACS Nano, 11, 9303 (2017)
Challenges for Area Selective Deposition

- Surface preparation
  - Incoming defects on non-growth surface
- Non growth area changes during deposition
  - Surface functionalization/modification during the ALD deposition
- Finite selectivity
- Slow/Throughput
- Defectivity and defect removal
- Metrology and characterization

Incoming surface is not clean so nucleation sites during ASD

Can defectivity in selective deposition be controlled?
Correction Step/Defect Removal

**Area selective deposition and etching**

**Al$_2$O$_3$ Dielectric Film**

- 48 hours of ODP deposition
- Al Auger map
- SEM: 60 cycles Al$_2$O$_3$ ALD after etching
- Cu, SiO$_2$
- 6.8 nm Al$_2$O$_3$
- SEM: 80 cycles Al$_2$O$_3$ ALD after etching
- Cu, SiO$_2$
- 9.4 nm Al$_2$O$_3$
- SEM: 100 cycles Al$_2$O$_3$ ALD after etching
- Cu, SiO$_2$
- 12.1 nm Al$_2$O$_3$

**Re-dosing Dodecanethiol Inhibitor Layer**

- Regenerate the inhibitor layer in vapor for 30 sec
- Auger Zn map
- Growth rate: 1.8 Å/cycle

- No re-dosing of DDT SAM: Gradual loss of selectivity
- Re-dosing of DDT SAM: Maintained selectivity

- Re-dosing process results in selective deposition of 3x thicker dielectric films
- Improved selectivity on patterned structures


Improved Selectivity using correction steps
Metrology and Characterization

- Blanket studies necessary to understand growth mechanism and loss of selectivity
  - Structural properties of the deposited films
  - Surface coverage and selectivity numbers
  - XPS, FTIR, RBS, SIMS….

- Develop metrology for relevant structures with scaled dimension

- Defectivity
Summary
Patterning paradigm towards placement accuracy

Top-Down Lithography

Shorter Wavelength
- Immersion
- EUV
- i-line
- KrF
- ArF

Multiple Patterning
- LEx
- Shrink
- SAMP

Self-Alignment
- Atomic Level Approach
- Multi Color Approach

Bottom-Up Lithography

Self-Alignment + Self-Assembly
- Selective Deposition
- DSA

The paradigm is expanding to self-alignment and bottom up approach
Summary

- 3D architecture and scaling are key requirements for sub 7nm generation
- Scaling booster along with aggressive pitch scaling will enable the next generation scaling
- EPE is the fundamental challenge for advanced patterning
- Patterning paradigm is expanding to self-alignment and bottom up approach
- Selective deposition will be an enabling technology in reducing complexity in advanced patterning as well as the increasing cost associated with it.
- Defects removal and metrology are key challenges that need to be addressed
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Thank you for your attention!