Selective CVD Metal Deposition for nano device in semiconductor fabrication

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Nano Copper Low K Interconnect BEOL Research: Unit Processing
Outline

- Introduction
  - Cu-Low k interconnect reliability enhancement with metal cap
  - Selective CVD Metal Deposition technology- INDUSTRY FOCUS ON device Capacitance reduction and reliability improvement.
- Selective metal CVD deposition processes : Focus on Co
- Selective Co Deposition applications in device fabrication
  - Wrap around metal cap for enhanced Cu BEOL reliability
  - Air Gap fabrication: Self align etch stop and reliability
- Other Selective metal CVD deposition processes : Ru, Pt, Mn
- Summary

Acknowledgments: This review also included contributions of numerous members of IBM metal teams, PFA, unit processes, equipment vendors and Harvard university’s Roy Gordon group. The contributions from C. Yang, H. Shobha, D. Priyadarshin, C. Penny, B. Briggs, T. Standaert and D. Canaperi are especially acknowledged.
Cu Barrier Cap in IBM’s sub-20 nm Cu-low k interconnect

- Prevent inter/intra level Cu diffusion into ILD dielectrics
- MUST shut down Cu diffusivity at top surface for EM reliability
- Act as a barrier to humidity ingress
- Act as an etch and CMP stop layer
- Good electrical properties with high breakdown to provide chamfer benefit
- Stress balance at the Cu low-k interconnect interface
  - Preferable cap with compressive stress to compensate for tensile stresses in ILD
- Good conformality to fill Cu divots
- Minimize impact on BEOL capacitance

SiN \((k=7)\) was replaced with SiCNH \((k=5.3)\) at 90 nm node and then thinner and lower k cap at <45 nm nodes. Selective metal (Co) cap introduced at <=14 nm nodes.

Contribution to interconnect capacitance becomes important as device dimension decreases

Presence of dielectric cap alone contribution up to ~ 17% of $C_{\text{Total}}$

- C reduction strategy for cap: reduce thickness and k value
  - evaluating lower k, thinner SiN/SiNO cap (k ~ 4.5-5, film thickness 10-12 nm)
  - ultra-thin SiCN or SiCN/SiN or SiNO with thickness ~ 8-10 nm
  - reducing dielectric cap thickness up to ~7 nm in combination with selective Co
# SiN/SiNO, SiCN Dielectric Caps Summary

<table>
<thead>
<tr>
<th>Scorecard Parameters</th>
<th>Ultra-thin Dielectric Cap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SiN/SiNO</td>
</tr>
<tr>
<td><strong>Oxidation Barrier Thickness (Å)</strong></td>
<td>100Å (min tested)</td>
</tr>
<tr>
<td><strong>Cu Barrier Thickness (Å)</strong></td>
<td>&gt;100Å</td>
</tr>
<tr>
<td><strong>Electrical Breakdown/Leakage @ 2MV/cm</strong></td>
<td>9 MV/cm / 2E-8 A/cm²</td>
</tr>
<tr>
<td><strong>Dielectric Constant</strong></td>
<td>~4.5-5</td>
</tr>
<tr>
<td><strong>Modulus (GPa)</strong></td>
<td>93</td>
</tr>
<tr>
<td><strong>Stress</strong></td>
<td>Compressive (as-dep and post UV)</td>
</tr>
<tr>
<td><strong>Conformality</strong></td>
<td>Highly Conformal</td>
</tr>
<tr>
<td><strong>Deposition Rate</strong></td>
<td>~30-40 Å/min (ok for thin cap)</td>
</tr>
</tbody>
</table>


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Cu-Cap Interface and its Impact on Electromigration

- Activation energies for Cu interconnects
  - bulk diffusion 2.3 eV
  - grain boundary diffusion 1.2 eV
  - interface diffusion 0.7-1.0 eV

- Interface diffusion having lowest activation energy is the fastest diffusion path for copper interconnects

- For damascene integrated copper, the two Cu interfaces are with liner and barrier cap
  - metal liners have good adhesion to Cu
- Better adhesion between the Cu and barrier cap reduces void growth rate and lengthens EM lifetime

Metal capping prevents fast Cu diffusion path at top surface

- Significant improvement compared to dielectric caps (SiN or SiCHN)

C. K. Hu, et al. 1-3

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Why CVD selective metal cap deposition?

- **Process:**
  - High quality conformal ultrathin (1-5 nm) enabling sub-10 nm Cu interconnect.
  - Low defect and compatible to vacuum environment. Low FM. Better thickness control.
  - Good process reproducibility with low pattern/dimensional sensitivity.
  - Can be in-situ integrated with other dielectric CVD in vacuum environment to minimize/eliminated unwanted/uncontrolled metal cap oxidation-enabling thinner metal cap.
  - Potentially more friendly to environment: Less chemical use. Volatile CVD precursors can be scrubbed more readily in current fab exhaust system.

- **Integration:**
  - No wet chemical or PVD processing minimize the adjacent insulator (ULK) damage or unwanted solvent diffusion into porous ULK (pSiCOH).
  - Robust ultra thin metal enable better Cu resistance: **Thicker Metal Caps by other process may take up Cu volume → increase Cu resistance nano Cu interconnect.**
Cyclic Processes for either nanolayers SiN dielectric or selective Co cap deposition on Cu/pSiCOH ULK

- Both of SiN and Co Cap deposition deposit by multilayer Cyclic deposition process with either Nitrogen or NH3 treatment steps between each thickness cycle
- Nanolayer process improves conformality of SiN.
- Nanolayer process enhances step coverage, selectivity and carbon content of Cobalt

N2 or NH3 Plasma treatment and densification

Ch A

Nanolayer (6A Co or 20A SiN) deposition

N2/NH3 plasma treatment to densify SiN cap (or densify and remove Carbon in Co layer)

Next Chamber

Next step (integrated) or wafer remove

After desirable thickness reach

Integrated CVD Equipment for Cyclic In-situ selective Cobalt and dielectric cap deposition

- SiH4 + NH3 used in Plasma CVD/ALD Nano SiN layer deposition + N2 plasma treatment at 350 C
- Cobalt carbonyl cyclopentadiene precursor is used for selective Co deposition at 210C

H2 Thermal Preclean of Cu with Hydrogen

CVD Co (210 C Thermal H2 PC) followed by cyclic Co dep and NH3 plasma treatment damage to ULK

350 C Thermal PC + Dielectric Cap
- Cyclic conformal multilayer SiN Cap,

Integrated In-situ Selective Co Metal Cap Process (Nguyen et al. ALD 2013)

Plasma treatment step in Selective Co deposition has negative impact to ULK → increase overall C

Select Co/Dielectrics Cap Process Sequence

Integrated process with NO air-break

Cu surface pre-clean in Ch A

Selective Co metal cap deposition in Ch C (plasma)

Dielectric barrier cap deposition in Ch A or Ch B

Conformal dielectric barrier film on top of selective Co to fill the divots

Wrap around structure

Selective Co Cap

Co Liner

Good divot fill

Conformal SC6 SiN Cap

Selective Co Deposition Process

- Thin (~6Å) of Selective Co dep
- NH3 Plasma treatment to generate fresh metal surface for high selectivity
- In-situ dielectric cap deposition
- Repeat cycles
- More plasma treatment steps for thicker Co

Selective Co Deposition Process

- Carbon depletion in near surface of pSiCOH ILD due to damage caused during Co deposition

- Table:
  - Ion
  - Mass
  - Color
  - C 12.00
  - SiN 41.98
  - Siz 55.95
  - SiC 59.97
  - Co 74.95

- Graph:
  - Graph showing capacitance and resistance for different Co thicknesses:
    - 30Å Co
    - 24Å Co
    - 12Å Co
    - No Co

Selective Co deposition causes damage to the underlying ULK

- Increase in capacitance with selective Co process observed
- Damage depends on type of ULK and can lead to potential degradation in TDDB

Low K Dielectric Repair Process for Capacitance Recovery

ILD Repair Process
Silylation in presence of UV

Non-integrated process

Integrated process

Damaged ILD layer

Post ILD etch

Post Co Cap

Post Repair + Dielectric Barrier

Co Metal Cap

Wafers move from RIE chamber → repair → liner/barrier deposition

Wafer transfer in a single tool from Co deposition → repair → dielectric barrier deposition

ILD Repair Process Results

- Selective Co deposition depleted carbon in near surface region of pSiCOH k 2.55
- UV repair in presence of silylation chemistry restored carbon in the film

Lateral growth in thick selective Co deposition - overgrowth issue

IMEC, 2nd Workshop in Selective Dep, 2017 and Ben Briggs et al, IBM
EM/TDDB Device Reliability: Integrated in-situ Selective Co/Cyclic SiN

- Selective Co improves the adhesion interface between Cu and dielectric cap
- Complete wrap around structure with Co cap and Co liner provides optimum benefits

- TDDB failure probability on low k pSiCOH k 2.55
  - No degradation in selectivity, results comparable to dielectric only barrier film without Co

Activation Energy Results: Selective Co Cap/Co Liner

- Line-depletion studies at 340C, 370C and 400C with selective Co cap/Co liner
- ~100X median failure times with wrap around structure over TaN/Ta – Dielectric barrier scheme

Wrap around Co cap/Co liner structure offers substantial EM improvement

TaN / Ru liner and in-situ selective Co & SiCN/SiNO cap

- No galvanic attack of Ru during Cu plating.
- Co diffuses from top interface, along Ru/Cu interface, into Ru.
- Excellent electromigration at 7 nm node.

36 nm pitch EM: V1 → M1

<table>
<thead>
<tr>
<th>Activation Energy</th>
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</thead>
<tbody>
<tr>
<td>Without Co cap</td>
<td>~0.85 eV</td>
</tr>
<tr>
<td>with Co cap</td>
<td>~1.5 eV</td>
</tr>
</tbody>
</table>


T. Standaert et al. IEDM 2016
Selective Co/Advance Dielectric Cap Summary

- Wrap around Co Cap shows 1000X EM improvement without TDDB degradation
- Ultra-thin dielectric cap: SiN/SiNO (low k, conformal) and SiCN (single layer) show robust barrier properties with good device reliability with lower capacitance
- Co process improvement in combination with low k, thin dielectric cap for further reduction in BEOL capacitance

Priyadarshini, Nguyen...IITC 2014/2016
IBM Air Gap at 65 nm Node

No new materials! Gap formation after each Cu level is completed.
Process Overview - Application of Selective Co in 48 nm BEOL pitch Air gap

1. Post CMP

2. Selective CVD Co Cap, Hardmask, and Resist Deposition

3. Etch and Wet for Air Gap Formation and Hardmask Removal

4. Conformal Dielectric Liner and Dielectric Cap

Airgap formation demonstrated at 48nm pitch with selective Co cap deposition
Airgap process has been optimized to eliminate erosion of the copper line
(C. Penny… Nguyen, IITC Conference 2017)
Process Overview – Improvement with selective Co for Air Gap

Co cap retention is a key element for achieving acceptable electromigration
Wet process optimization enabled formation of airgap while retaining Co cap

Selective CVD of Ru Cap for Cu_low K interconnect

Ru$_3$(CO)$_{12}$ was used in Ru cap deposition at 200 C

70 nm Cu_ULK line and space Structure. Good EM improvement

Selective Sidewall Pt deposition in Si Fin with CFx implantation

3D AS-ALD of Pt Thin Films on Selectively CF\textsubscript{x}-Implanted Si 3D Fins

Schematic illustration of 3D AS-ALD of Pt thin Films on Si Fin Arrays

Cross-sectional TEM images of Si fin arrays with deactivated horizontal surfaces

Successful demonstration of topographically selective growth of Pt thin films along vertical sidewall !!

Stanford University, Department of Chemical Engineering

Woo-Hee Kim et al., ACS Nano, 10 (2016) 4451–4458
Ultrathin Mn/Ru liner will need Mn Cap for Mn wrap around Cu

- 1nm Mn / 1nm Ru liner scalable down to 16nm width
  - Line height roughly fixed in analysis below.
  - C effectively increasing.

M. van der Veen, et al.\textsuperscript{1}

B/L thickness scaling is not enough to further lower $R_{BEOL}$ for CD $< 16$nm

\textsuperscript{1}M. van der Veen, et al., IITC/AMC 2016;

T. Standaert et al. IEDM 2016
CVD thin Mn form MnOx (remove O in Cu surface) → enhance Cu-dielectric adhesion and EM

Issues of current dielectric (SiCN) capping layer

• Sub 30 nm Cu and SiCN cap interfaces
  → Low electromigration resistance
• Need non plasma CuOx removal
  → No plasma damage on p-SiCOH

Mn self-aligned capping layer- Our focus on Cu-cap surface and MnOx-pSiCOH ILD

Cu/CVD Mn(sel. prefer)/Dielectric+ anneal

=> Good Cu adhesion to insulator cap
=> No dielectric-Cu interfaces in this case.

Dielectric-Mn/MnOx-Cu interface formation
→ Improve EM

Chemical Vapor Deposition of Manganese

Precursors: Manganese and SAM

SAM=Self Assembly Monolayer
(mostly Carbodisilane molecules) are used for surface treatment (prior to Mn deposition) to increase Mn deposition selectivity on Cu (vs p-SiCOH 2.2/2.4).
SAM1=\(N,N\)-Dimethyltrimethylsilylamine (C5H15NSi)
SAM2=Bis(dimethylamino)dimethylsilane (C6H18N2Si)

Name: \(\text{bis}(N,N'\text{-diisopropylpentylamidinato})\) manganese(II)
Melting Point: \(~60^\circ \text{C}\)
Vapor Pressure: \(~0.1\ \text{mbar at 90}^\circ \text{C}\)

CVD System Set up at Harvard for selective Mn deposition on Cu- Selectivity improved (30-40x higher, Cu/p-SiCOH :200-1000) with p-SiCOH/Cu pattern expose to SAM prior to deposition

1) No Plasma Treatment step, No ULK damage
2) Precursor has No Oxygen→ No Liner oxidation

Selective Mn deposition experimental set up
(Nguyen…Gordon, Au.. Et al. , Proceed. ALD July 2015)
Capping Layer Application of CVD-Mn

Typical XPS analysis of Mn selective deposition with surface passivation using self-assembling monolayers (SAM)

Very High Mn selective is observed On Blanket Cu/SiO2-SiCOH film

Procedure
Reduction with Hydrogen
Surface Passivation with SAMs
CVD-Mn Deposition
Process optimized for 90 nm pitch
Cu_pSiCOH k2.2
(Nguyen..., Gordon, Au et al. ALD 2015..)

Selectivity over 200:1 can be achieved

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Mn Atoms</th>
<th>Selectivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 PVD-Cu</td>
<td>1.45x10^{16}</td>
<td>--</td>
</tr>
<tr>
<td>2 Thermal Oxide</td>
<td>&lt;5x10^{13}</td>
<td>&gt;290:1</td>
</tr>
<tr>
<td>3 p-SiO_2</td>
<td>&lt;5x10^{13}</td>
<td>&gt;290:1</td>
</tr>
<tr>
<td>4 Low-k pSiCOH k 2.2-2.7</td>
<td>~7x10^{13}</td>
<td>207:1</td>
</tr>
</tbody>
</table>
Detailed views of the surface of two of the structures near the edge of the lines. The Mn deposition is clearly present on top of Cu and none p-SiCOH 2.2, though apparently thin Mn in the indicated location (oval).

**The expected Mn thickness is 2.5 nm, the TEM measured Mn thickness is ~3 nm**

( Nguyen... Gordon, Au et al., ALD 2015)
TEM/EDX/EELS analyses of Selective Mn deposition on 32 nm M1 Cu-p-SiCOH 2.2 pattern structure

Similar EDX/EELS maps were obtained at the edge of a line, over the low-k surface (red rectangle in STEM image at left). Maps at right show no indication of Mn over the ULK or over the Ta liner, only over the Cu surface. **EXCELLENT CVD Mn selectivity on Cu confirmed.**

( Nguyen..., Gordon, Au et al., ALD 2015 Proceeding )
Selective Mn will form complete Wrap around with SFB Mn Liner

SFB Mn metal Cap

EELS shows Mn accumulation across entire Cu/NBLOK interface, and curving over into liner interface

The left side has no indication of Mn at the Cu/liner interface.

The right side has indication of Mn and O at the same time.

PVD asymmetry created a thinner TaN on the right side where Mn accumuliated to trap oxygen which invaded from low-k to copper.

Cu Mn IBM Scheme (Nogami). CVD Mn/MnNx will eliminate the need for CuMn (2-10 % Mn) seed in Self Forming Barrier (SFB) scheme that impact resistance greatly. CVD MnSiOx/MnSiCOH, and MnNx also show promising barrier potential... that minimize the negative impact of litho/etch profile and dimension control variability. With the self-limiting reaction, the SFB enable 1-2 nm liner thickness. In SFB approach, Mn concentration in Cu can be high (2-10% wt) and negatively impact (increase) Cu resistivity. NEED better Mn SFB source

Manganese Scabbing Model

Blood platelet reacts on oxygen in the air to form scab on our skin, when injured. Mn reacts on oxygen at the surface and at defects to form MnO.

Cu Top Surface

Locally too thin Ta

Defective Interface

Nogami et al., IEDM Proceeding, p.33.5.1 - 33.5.4. 2010

Mn makes perfectly coated Cu lines → Excellent EM performance
Feasibility Study: **Selective Mn deposition on 90 nm pitch Metal 1 chip**

200A (20nm) Mn deposited at 300 C with ½ hour ramp up and down-Chip passivated with 150A PECVD SiNx

The Mn deposition selectivity of un-passivated on p-SiCOH (2.2/2.4) over Cu are 4:1 and 25:1 respectively

The Mn deposition selectively on Silicon-based SAM on p-SiCOH (2.2/2.4) over Cu are higher (200-1000 range)

### Low Leakage but ~20% increase in Cu resistance for Thick 20 nm Mn

<table>
<thead>
<tr>
<th>Device</th>
<th>Initial Resistance (ohms)</th>
<th>Initial Leakage (amps)</th>
<th>Resistance after Heating (ohms)</th>
<th>Leakage after Heating (amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>REMONCD</td>
<td>459,900</td>
<td>4.43E-09</td>
<td>568000</td>
<td>1.00E-06</td>
</tr>
<tr>
<td>REMONAB</td>
<td>482,700</td>
<td>5.36E-09</td>
<td>619950</td>
<td>3.54E-09</td>
</tr>
</tbody>
</table>

Leakage @ 5 volts

Resistance measured @ 10 microamps

Selective Mn deposition on Cu reduce the Cu line to line leakage

Cu resistance increase due to Mn diffusion into Cu.

Need additional optimization

Mn Diffuse into Cu and increase resistance

Need to reduce the amount of Mn deposited

Nguyen…Gordon, Au et al., ALD 2015 proceeding)
CVD – Mn form MnSiOx and maintain low leakage of insulator MnSiCxOy or MnSiCxNyOx may have same performance (R. Gordon et al., Vapor Deposition of Materials for Microelectronic Seminar, 2012)
Mn Diffusion in pSiCOH: OMCTS Ex k 2.55, 2.4

Depth of penetration of the Mn by XPS (1nm/level):

- Mn amidinate precursor used for Mn deposition on OMCTS Ex film → no significant penetration of Mn detected in this ILD material
  - Pores in OMCTS Ex smaller than amidinate precursor and prevents diffusion of Mn in low k
  - Other types of pSiCOH ULK 2.4 showed significant Mn penetration
  - UV curing the surface prior to Mn deposition makes the surface hydrophilic – some Mn detected in UV cured sample

Nguyen...Gordon, Au et al., ALD 2015 proceeding)
Typical resistance and leakage changes in 90 nm pitch Cu-pSiCOH k2.2 structures (~90 nm pitch) after various process/treatment steps of selective and evaporated (NON-SELECTIVE) Mn deposition

<table>
<thead>
<tr>
<th>Sample No</th>
<th>% (Pre-Post) 300C anneal Serp Resistance change</th>
<th>Comment</th>
<th>% (Pre-Post) 300C anneal Leakage change</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (0.5nm sel. CVD Mn)</td>
<td>(-1%)</td>
<td>Good</td>
<td>1.5%</td>
<td>Good, No change</td>
</tr>
<tr>
<td>4 (1nm sel. CVD Mn)</td>
<td>(-2%)</td>
<td>OK</td>
<td>2%</td>
<td>OK, no real change</td>
</tr>
<tr>
<td>5,7 (2.5nm sel. CVD Mn)</td>
<td>~1-3%</td>
<td>Small change</td>
<td>2-3.5%</td>
<td>minimal increase</td>
</tr>
<tr>
<td>A (20nm sel. CVD Mn)~10%</td>
<td>20%</td>
<td>Large increase</td>
<td>3.2%</td>
<td>Small increase</td>
</tr>
<tr>
<td>1A(0nm/H2/SAM/Cap)</td>
<td>1%</td>
<td>No change</td>
<td>(-1 to 2%)</td>
<td>No change</td>
</tr>
<tr>
<td>2B (0 nm, H2/Cap)</td>
<td>(-1.5%)</td>
<td>No change</td>
<td>&gt;(-2%)</td>
<td>No change</td>
</tr>
<tr>
<td>3A(0 nm, cap)</td>
<td>(-2.5%)</td>
<td>H2O outgas</td>
<td>~(-3%)</td>
<td>H2O outgas</td>
</tr>
<tr>
<td>NON-Selective (YKT)</td>
<td>Evaporated Mn (0.5,1,2,3 nm)-Whole wafers (patterned)</td>
<td>Non Selective Mnt</td>
<td>Almost all device has small leakage,</td>
<td>Non Selective Mn CVD cause small leakage. Required annealing</td>
</tr>
</tbody>
</table>

Selective Mn CVD processing steps:

1) H2= H2 reduction 250C for 1hr;
2) SAM= Self Assembly Monolayer TREATMENT for 90c, 30 min (SAM1=N,N-Dimethyltrimethylsilylamine (C5H15NSi), SAM2=Bis(dimethylamino)dimethylsilane (C6H18N2Si))
3) Selective deposition of Mn (0, 0.5, 1, 2.5 and ~20 nm) with bis(N,N'-diisopropylpentylamidinato) manganese(II)+ Hydrogen
4) Cap = Capping layer (~50 nm PECVD SiNx) deposited at 300 C

SELECTIVE Mn (0.5-2.5 nm) cap deposition cause minimal Cu resistance and leakage change in 90nm pitch Cu-pSiCOH k 2.2

Nguyen...Gordon, Au et al., ALD 2015 proceeding)
Self-aligned Mn/MnSixOyNz potentially enable sub-5 nm cap thickness and wrap around SFB Mn Liner/Mn Cap for sub-7 nm BEOL Cu-Low k

- Selectively deposit manganese on Cu wires to form a CuMn alloy
- Deposit capping insulator layer (Si₃N₄ or SiCN) on top
- Anneal to allow manganese to diffuse to the Cu/capping layer interface
- Manganese enhances adhesion at the interface and forms a self-aligned MnSiₓOᵧNₓ diffusion barrier

Summary

- Advanced ultra-thin metal caps are required to enhance electromigration reliability in sub-20nm Cu interconnects.

- CVD/ALD Selective metal deposition provides one of the best approaches to form selective metal cap on Cu interconnect with ultrathin cap that have superior reliability performance.

- Selective Co cap has been used as self-aligned etching mask and cap for 48 nm Pitch BEOL Air Gap fabrication with excellent reliability.

- Various selective CVD Cobalt, Ruthenium, Manganese caps were evaluated: Selective Co cap/Co liner (wrap around structure) on Cu shows the best EM improvement without any TDDB degradation in sub-20 nm Cu interconnect.

- Selective CVD Co is currently implement in industry Fabs.