TECHNICAL PROGRAM ABSTRACTS

Tuesday 4th June

Wednesday 5th June

Thursday 6th June

TECHNICAL PROGRAM: TUESDAY 4TH JUNE

Session 1 - Opening

Royal A and B rooms, 1st floor
Session Chairs: Robert Socha, *ASML*, Axel Preusse, *Global Foundries*

08:15 - 08:25
Welcome

08:25 - 08:35
2018 best paper awards

08:35 - 09-25
KEYNOTE - Lithography status for 3nm node and below
Martin van den Brink, *ASML*

Lithography is a key enabler in continuing the shrink in semiconductor manufacturing. In order to enable the shrink, a holistic approach is necessary. Holistic lithography delivers performance and control through integration of patterning, metrology, inspection, and modeling. In holistic lithography, there are three necessary components which are: the lithography scanner with advanced capability, computation lithography and metrology, and optical and E-beam metrology. The lithography still delivers the necessary imaging, overlay, and focus needed for the advanced nodes. In addition to this advanced capability in the scanner, there are three holistic components which are: process window enhancement, process window control, and process window detection. In process window control, computation lithography and metrology is used to optimize the scanner to deliver the largest process window possible. In process window control, the optical and E-beam metrology is used with feedback and control software to maintain the process window delivered by the scanner. And in process window detection, computation lithography and metrology instructs where the optical and e-beam metrology should measure; thus, improving the effectiveness of the metrology and reducing the measure and acquire time of the metrology.

In addition to holistic lithography, another focus of this presentation is on the status of extreme ultraviolet (EUV) lithography. EUV requires fewer lithography and etch steps; thus, EUV is more cost effective. The cost effectiveness of the ASML EUV NXE (NA=0.33) and EXE (NA=0.55) platforms will continue to drive scaling beyond the next decade. The current EUV NXE:3400B scanner is capable of 125 wafers per hour. With this wafer per hour capacity, EUV is now being used in high volume manufacturing.

09:25-10:15
KEYNOTE - Integration across all levels of the system: the future of high performance compute SOCS
Mark Fuselier, *AMD*

As the use cases and usage statistics continue to expand exponentially for AI, Machine Learning, and Big Data, our traditional tools to scale computing performance and bandwidth are slowing. The solution: Drive scaling across all dimensions of the solution space -- chip interconnect, bump and package interconnect, multi-chip integration at package level, and PCB scaling for power/performance – to continue the power/performance scaling into the sub-10nm generation. New solutions in power distribution, extrinsic defect yield detection and elimination have been fundamental to overcoming the challenges with new and more aggressive on-chip interconnect materials and integration schemes. As heterogenous and high bandwidth package interconnects have challenge package signal routing, bump and substrate interconnect scaling have been required to overcome die area scaling constraints. New packaging solutions have arisen to allow for mixed-use chip integration outside of the now costly monolithic SoC approach. Even advances in PCB parasitics has been recently required to advanced system level performance. Putting all of these solutions together into an integrated System scaling approach is required to enable the future of high performance computing.

10:15 - 10:35
AM break

Session 2 - Advanced Interconnect

Royal A and B rooms, 1st floor
Session Chairs: Dan Edelstein, *IBM*, Kaushik Kumar, *TEL*

10:35 - 11:05
2.1 INVITED - Future metallization strategies for scaling and Improving Interconnect performance
Christopher J. Jezewski, *Intel*

Reducing interconnect resistance and capacitance is paramount to delivering performance in future technology nodes [1]. In order to enable more devices per unit area, the interconnect stack needs to include an ever increasing number of materials and layers. The pitch of the local interconnect layers needs to scale with critical device dimensions, which results in an intrinsic interconnect degradation in resistance/capacitance and current-carrying capabilities that need to be overcome with process improvements.

The last two major metallization changes are the introduction of Cu (replacing Al) to reduce resistivity, and Intel's recent introduction of Cobalt as local interconnect for the 10 nm node [2]. Cobalt has excellent gapfill, better electromigration performance than Cu, and requires thinner barrier/liners, which improves via resistance and partially mitigates its intrinsic higher resistivity than Cu [2]. Other alternative metals to Cu that have been proposed and investigated include Ru, Mo, and binary compounds. These materials have shorter electron mean free paths than Cu, and are therefore expected to have lower resistivity increases with scaling dimensions due to size effects. For any given metal and interconnect pitch, a known way to improve interconnect resistance is to increase conductor area by decreasing barrier/liner thickness, which requires thinner conformal novel barriers/liners. An effective way to reduce capacitance is to introduce structured porosity in the form of airgaps, which have been implemented in recent technology nodes [3].

In this paper, we will discuss requirements and opportunities for interconnect improvements, highlight critical research areas, as well as emerging candidates for metallization, including barrier/liner and conducting metal. In addition, we will describe the use of electromigration and biased thermal stressing quick-turn monitors that enable rapid exploration without the need for fully integrated stacks, not widely available in Academia [4]. Lastly, we will discuss selective deposition processes being proposed to simplify or assist interconnect processing, including metal-on-metal and metal-on-dielectric processes [5]. Special emphasis will be given on addressing defect tolerance and film quality in regions with both selective and nonselective materials present.

11:05 - 11:30
2.2. Co and Ru Dual Damascene Compatible Metallization Studies
Marleen H. van der Veen, N. Heylen, S. Larivière, V. Vega Gonzalez, E. Kesters, Q.T. Le, L. Teugels, S.A. Chew, H. Philipsen, J. Hung*, C. Adelmann, K. Vanstreels, N. Jourdan, F. Holsteyns, H. Struyf, C.J. Wilson, Zs. Tőkei, * *Nova Measuring Instruments, LTD, P.O. Box 266, Weizmann Science Park, Rehovot 76100, Israel, imec, Kapeldreef 75, B-3001 Leuven, Belgium*

This paper discusses challenges in the dual damascene metallization based on full Co and full Ru fill. Cobalt is a corrosive material and its loss is minimized during the clean and CMP by using alkaline chemistries. The corrosion potentials for Co coupled to TiN are linked to the narrow line corrosion that is seen at the Co CMP clear step. So far, Ru dual damascene metallization is hampered by the availability of a CMP process. We show an optimized CMP process for Ru in 34nm pitch structures with a nonuniformity of < 7nm, giving leakage-free structures, and that is scaleable to 10nm wide lines. The defects are lowered using a 1nm TiN liner on SiO2 and a combination of a hard and soft pad Ru polish step. The Ru-on-Ru via resistance is benchmarked to Cu and Co, and is 4x lower than Cu. This makes barrierless Ru vias viable candidates for advanced nodes.

11:30 - 11:55
2.3. Co Reflow and Barrier Scaling Studies for Beyond 7 nm Node BEOL Applications
P. Bhosale, S. Parikh*, R. Shaviv*, N. Lanzillo, G. How*, M. Stolfi*, L. Jiang, W. Du*, R. Tao*, G. Lam*, R. Conti, J. Kelly, and B. Haran, *IBM Research, Albany, NY 12159, *Applied Materials Inc., 974 East Arques Avenue, Sunnyvale, CA 94085*

Co interconnect performance for beyond 7 nm node (B7 nm) BEOL applications was investigated in terms of effective resistivity (ɣ: resistance and trench area product) and power vs freq. curves. The ɣ for Co at minimum pitch was comparable to the electroplated Cu and 1.4x of theoretical Cu performance. The performance improvements were achieved through barrier scaling (7 Å TiN/ 10 Å TaN) and Co fill optimization using novel Co reflow processes. These processes were developed using combination of CVD (chemical vapor deposition), PVD (physical vapor deposition) Co deposition and in-situ thermal anneal. Simulation results show that the thinner barrier reduces via R by as much as 60%. Lower line and via R were also predicted to improve the device performance gain by 6% on a standard cell design with high via density.

11:55 - 12:20
2.4. Novel Volatile Film for Precise Dual Damascene Fabrication
M. Fujikawa*, T Yamaguchi*, S. Nozawa*, Y. Kikuchi1, K. Maekawa|1, H.Kawasaki
**S-Technology Development Center, Tokyo Electron Technology Solutions Limited, 1Module Integration Group / TEL Technology Center, America, LCC*
Process Integration Center / Tokyo Electron Limited

Plasma induced damage on porous low-k dielectrics is a critical issue to lower the interconnect RC delay in the latest and upcoming highly dense integrated circuits. In order to reduce the exposure the low-k material to plasma, a novel volatile material, which can be removed simply by thermal energy is developed [1]-[6]. Utilizing this film as temporary sealing plug, it can protect the low-k dielectrics from being exposed to plasma during upcoming ashing processes, and furthermore. It can be removed easily without additional damage. In this paper, we demonstrate the effect of the volatile material by examining its filling property, electrical characteristics and reliability on the test pattern.

12:20 - 12:45
2.5. Interconnects for scaled SRAM with vertical Surrounded Gate Transistors (SGT)
J. Bömmels1, N. Harada2, M.-S. Kim1, J. Mitard1, Y. Kikuchi1, W. Li1, Z. Tao1, H. Puliyalil1, K. Devriendt1, C. Lorant1, Q. T. Le1, E. Kesters1, N. Jourdan1, Z. El-Mekki1, L. Teugels1, M. H. van der Veen1, Y. Li2, H. Nakamura2, D. Mocuta1, F. Masuoka2, *1imec, Kapeldreef 75, 3001 Leuven, Belgium*
2Unisantis Electronics Singapore Pte Ltd, 10 Science Park Rd. #03-17A The Alpha Singapore Science Park Ⅱ, Singapore

A interconnect scheme for vertical Surrounded Gate Transistors (SGT) is described. Key features are a buried connection between bottom side and gate, a self-aligned scheme of Top Electrode and Via to Gate, and the use of Supervias to mitigate the minimal islands

12:45 - 14:00
Lunch

Session 3 - Beyond Copper I
Royal A and B rooms, 1st floor
Session Chairs: Stefan Schulz, *TU-Chemnitz and Fraunhofer ENAS*, Kaoru Maekawa, *TEL*

14:00 - 14:30

3.1. INVITED - Metallization Challenges in 3D NAND Flash Memory
Raghuveer Makala, *Western Digital*

As 2D planar NAND flash memory scaling became increasingly difficult and cost-prohibitive, 3D NAND architecture emerged as a viable alternative. Thin film deposition in complex geometries and

Reactive Ion Etching of multilayer stacks has been pivotal in enabling high yield, low cost 3D NAND production. Continued development for future nodes will require revolutionary approaches due to increased loading densities and cost/bit density requirements. This talk discusses the challenges, potential solutions and future directions in a gate-last approach for 3D NAND metallization.

Due to its thermal stability and excellent electric conductivity at small dimensions, tungsten (W) is widely used for both front-end and back-end metallization in the semiconductor industry. In Charge Trap 3D NAND, W control gates or Word Lines (WL) are formed by a replacement process. However, uniform deposition of barrier layers and nucleation films and void-free gap-fill is not a trivial problem in complex geometries and aspect ratios that routinely exceed 50:1. Meanwhile, 3D NAND extendibility requires W-WL thickness reduction so that total stacked pairs or memory layers can keep increasing over future technology nodes, while meeting acceptable levels of sheet resistance. This makes it even more difficult for gap-filling in sideways recessed 3D fins with shrinking dimensions. In addition, severe wafer warp associated with the increased volume of W, imposes limitations on the number of 3D layers that can be fabricated. Moreover, residual fluorine in the WLs from the WF6 precursor diffuses into inner dielectrics and creates reliability problems -making WL metallization a very key technology that determines 3D NAND scaling.

In this talk, we will review the metallization challenges faced in recent 3D NAND nodes, lessons learnt and the upcoming challenges as we continue 3D NAND scaling for the years to come. This talk will discuss some of the promising technologies for lowering WL resistance, controlling fluorine content and stress management that include: ALD deposition, incubation delay, fluorine-free barriers/films, and touch upon alternative metals for future generations.

14:30 - 14:55

3.2. Replacing TaN/Ta Bilayer with 2D Layered TaS2 Converted from Ta for Interconnects at Sub-5 nm Technology Nodes
Chun-Li Lo1, Han Li2, Wanying Ge4, Carl H. Naylor3, Xunhua Zhao4, Yuanyue Liu4, Kevin L. Lin3, and Zhihong Chen1*
1 School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907, USA, email: zhchen@purdue.edu 2 Technology Manufacturing Group and 3 Components Research, Intel Corporation, Hillsboro, OR, USA 4 Texas Materials Institute and Department of Mechanical Engineering, The University of Texas at Austin, Austin, TX, USA

Two-dimensional layered TaS2 with ~1.5-nm thickness is developed to replace the conventional TaN/Ta bilayer stack (> 4 nm) in order to maximize Cu volume and reduce via resistance for next-generation interconnect technologies. The TaS2 ultra-thin film, unlike most of the proposed 2D barriers, is industry-friendly, back-end-of-line-compatible, and can be directly deposited on dielectrics. Our results show this ~1.5-nm TaS2, serving as both the barrier and liner, would enable continued scaling of interconnects beyond 5-nm-node

14:55 - 15:20
3.3. Circuit Delay and Power Benchmark of Graphene against Cu Interconnects
Antonino Contino∗†, Ivan Ciofi†, Rogier Baert†, Xiangyu Wu∗†, Inge Asselberghs†, Umberto Celano†, Christopher J. Wilson†, Zsolt Tokei†, Guido Groeseneken∗† and Bart Soree∗†∗*KU Leuven, 3001 Leuven, Belgium, †Imec, 3001 Leuven, Belgium*

In this paper we benchmark various graphene interconnect schemes against Cu metallization in terms of circuit delay and power, based on device and wire-load assumptions representative for the 3 nm logic technology node. Graphene and Cu performance are evaluated using models calibrated to experimental data. In our study, we vary the number of graphene layers, the number of metal layers implementing graphene and the graphene contact resistance to the nearby metal layers. We show that up to 12% delay reduction (16% for the best contact resistance) can be achieved at lower power consumption. Alternatively, 21% (34% for the best contact resistance) of power reduction can be achieved for the same delay of Cu by modifying the graphene interconnect configuration

15:20 - 15:45

3.4. 21 nm Pitch Dual-Damascene BEOL Process Integration with Full Barrierless Ru Metallization

V. Vega-Gonzalez, C. J. Wilson, S. Paolillo, S. Decoster, M. Mao, J. Versluijs, J. Bekaert, V. Blanco, E. Kesters, Q.T. Le, C. Lorant, O. Varela Pedreira, A. Leśniewska, N. Heylen, Z. El-Mekki, M. van der Veen, T. Webers, H. Vats, L. Rynders, M. Cupak, J. Uk-Lee, Y. Drissi, L. Halipre, A.-L. Charley, P. Verdonck, T. Witters, S. V. Gompel, Y. Kimura, N. Jourdan, I. Ciofi, A. Contino, G. Boccardi, S. Lariviere, B. De-Wachter, E. Vancoille, F. Lazzarino, M. Ercken, R. Kim, D. Trivkovic, K. Croes, P. Leray, I. Grisin, K. Pardons, D. Mocuta, G. McIntyre, K. Barla, Z. Tokei.
imec vzw, Kapeldreef 75, B-3001 Leuven, Belgium.

A dual-damascene (DD) 21 nm metal pitch (MP) test vehicle relevant for the 3 nm logic technology node (N3) was designed and fabricated to explore patterning and metallization. A full barrierless ruthenium (Ru) metallization and an intermetal insulator with a relative dielectric constant k = 3.0 were implemented using self-aligned quadruple patterning (SAQP) based on argon fluoride immersion (ArFi) lithography, and extreme ultraviolet (EUV) lithography for patterning of blocks and vias. Lines and vias gave expected average resistance values of 340 Ω/µm and 15 Ω, respectively. No upstream electromigration (EM) failures were seen after 530 hours at 330 °C with a current density of 3 MA/cm2. Time-dependent dielectric breakdown (TDDB) tests confirmed a high acceleration factor (m = 20.84 ± 5.2) and a time-to-failure (TTF) > 10 years at 100 °C. The measured RC gave a 30% improvement compared to a calculated Cu reference at this node. This demonstrates full Ru integration as a viable process option for advanced technology nodes

Session 4 - Posters and Networking

Amsterdam – Luxembourg, 1st Floor

16:00 - 18:00

4.01. Stability of Cu Surface after post CMP Cleaning

Yasuhiro Kawase Toshiaki Shibata1, Tomohiro Kusano2, Ken Harada1 and Kan Takeshita2
Mitsubishi Chemical Corporation 1 Kurosaki R&D Center, Fukuoka, Japan 2 Yokohama R&D Center, Kanagawa, Japan
Mitsubishi Chemical Corporation Electronic Applications and Organic Materials Kurosaki R&D Center, Fukuoka, Japan

In advanced semiconductor manufacturing processes, over 10 layers of Cu interconnect have already been applied and application of Co for both plug and interconnect is being considered in most advanced technology node. In the process of post Cu chemical mechanical polishing (CMP) cleaning, it is necessary to remove not only abrasive particles but also organic residue derived mainly from CMP slurry without any corrosion. But in some situations after post Cu CMP cleaning, specific Cu or CuOx grain growth defects was observed at narrow line width especially <50nm. So we think over the surface stability of Cu after post CMP cleaning and would like to report the effect of the passivation due to Cu oxide

4.02. Elevated Temperature Self-Assembled Monolayer (ET-SAM) Barrier and its Characterization by Variable Bias Electrochemical Impedance Spectroscopy (VB-EIS)

Kian Kadan, Junyi Zhou, Yelena Sverdlov, and Yosi Shacham-Diamand
Department of Physical Electronics, School of Electrical Engineering and The Department of Material Sciences and Engineering, Engineering Faculty, Tel Aviv University, Ramat Aviv 69978, Israel

In this work, we present a feasibility study of ultra-thin organic barriers deposited at elevated temperatures for Ultra Large-Scale Integration (ULSI) metallization. We also demonstrate the feasibility of using Electrochemical Impedance Spectroscopy (EIS) for quick turnaround, inline metrology determining the SAM key parameters: coverage and average thickness. The novel process uses self-assembled monolayer (SAM) where new solvents with high flash point temperature were explored. The goal was to develop a safe deposition process at T>90°C using high flash-temperature solvents, e.g. N methyl-2-pyrrolydone (NMP, Tflash point=91°C) and Ethylene glycol (EG, Tflash point=116°C). Those high temperature solvents were tested as candidates to replace existing low-flash point temperatures solvent, commonly used today, such as toluene, ethanol and

IPA Three silane (Head group) based monomers were tested; each with 3 Carbon chain but three different tail groups: amine, aniline and methacrylate. Therefore, in addition to the solvent effects the tail group effects were also studied. The study present here describes a novel safe process, at temperatures above 90°C up to 150°C, compatible with fabrication sites safety roles allowing faster deposition time, in the range of 1- 10 minutes. Therefore, allowing higher deposition temperature (up to 150°C) yielding shorter deposition time, thus, allowing higher throughput. All three monomers yielded high quality uniform film on silicon, thermal oxide and Low-K dielectrics. Cu/ET-SAM barrier/Si structures were annealed in vacuum at 400 °C for up to an hour did not show any failure. The various layers were characterized by Electrochemical Impedance Spectroscopy (EIS) at bias ranging from -1.2V to +1V. The results were fitted to a model to determine the layers effective thickness and coverage. The films' properties have been also characterized by conventional surface science methods: contact angle (CA), spectroscopic ellipsometry (SE), X-ray Variable angle Photoelectron Spectroscopy (VA-XPS), and Atomic Force Microscopy (AFM) and Kelvin Probe Scanning Microscopy (KPFM)

4.03. Advanced Modeling and Simulation of Cu Nano-Interconnects Reliability
H. Ceric-a and H. Zahedmanesh-b
a-Institute for Microelectronics, TU Wien Gußhausstraße 27–29/E360, 1040 Wien, Austria b-imec, Kapeldreef 75, Leuven 3001, Belgium

The need to develop new interconnect technologies as devices scale below 10nm intro-duces new reliability challenges that need to be addressed by new models and modeling meth-ods. In this work, we present a complete model-ing framework that considers all relevant physical aspects of the reliability problem.

4.04. Investigation of Layout- and Process Dependence of Cu-ECD for advanced nodes
M. Wislicenus-1, L. Gerlich-1, J. Koch-1, B. Uhlig-1, J. W. Bartha-2, A. Preusse-3
1-Fraunhofer IPMS-CNT Dresden, Germany, 2-IHM, TU Dresden Dresden, Germany, 3-GLOBALFOUNDRIES Module One LLC Co. KG Dresden, Germany

Basic interactions between ultrathin Cu and Co based seed layers with low acid plating chemistry are studied in the context of advanced dual damascene metallization. Utilizing a variety of micro-analytical techniques this multi-scale investigation is focused on the layout and process dependent seed layer resistance and its impact on the Cu-ECD. A new method is used which permits micro-scale resistance measurements perpendicular to the trench direction showing high sensitivity to process modifications. Furthermore, structure dependent cross-wafer resistance measurements are used to identify both, layout induced seed resistance anisotropy as well as post plating copper distribution

4.05. A Study on Mechanism of SiO2-CMP Focused on Adhesion Force of Abrasive Particles
Shota Suzuki, Tomohiko Akatsuka, Akira Endou, and Kazumi Sugai
CMP Department, FUJIMI INCORPORATED 1-8, Techno Plaza, Kakamigahara city, Gifu, 509-0109, Japan.

Polishing slurries for SiO2-CMP have been found to specifically enhance the material removal rate for SiO2 under certain conditions. The extraction of its key parameter is indispensable to the further enhancement of the removal rate for SiO2. In this study, the key parameters to enhance removal rate for SiO2 were investigated on the basis of the consideration of the polishing mechanisms of SiO2. It was revealed that the most effective parameter was the adhesion force of abrasive particles to SiO2.

4.06. Investigation of chemical mechanical planarization (CMP) and post-CMP cleaning of Molybdenum
Ken Harada, Harold Philipsen-1, Lieve Teugels-1, Herbert Struyf -1
1-imec Kapeldreef 75, B-3001 Leuven Belgium , Mitsubishi Chemical Corporation Kitakyushu, Fukuoka, 806-0004, Japan

Molybdenum is a candidate material for various applications, such as interconnects and memory. Control of the surface oxidation state (type and thickness of oxide) is important. In order to establish chemical mechanical planarization (CMP) and a post-CMP cleaning process, surface analysis was

performed using X-ray photoelectron spectroscopy and atomic force microscopy. Coupon results for both an alkaline CMP slurry and post-CMP cleaning yield the most promising results that can be used as input to further develop wafer-scale processes.

4.07. Effect of SPS Addition for Electroless plating of CoB
Shusuke Shindo, Kosei Morita, Taro Matsudaira, Tomohiro Shimizu, Takeshi Ito, and Shoso Shingubara
Kansai University, Graduate school of Science and Engineering, Osaka, Japan

For ultra-fine LSI interconnections, high melting temperature metals are important candidates which take place of conventional Cu/barrier metal technology. This study focused on electroless plating of Co using dimethylamine borane (DMAB) as a reducing agent. We studied to possibility of bottom-up fill of CoB with addition of Bis(3-sulfopropyl)disulfide (SPS) as an inhibitor. It turned out that Co deposition rate was strongly suppressed with SPS concentration larger than 4.0 ppm, which suggested possibility of bottom-up fill in a fine via hole structure and fine trenches.

4.08. Ruthenium Recess for Buried Power Rail Integration
Anshul Gupta1, Jodi Grzeskowiak2, Nicolas Jourdan1, Kai-Hung Yu2, Nicholas Joy2, Shreya Kundu1, Lieve Teugels1, Jürgen Bömmels1, Christoph Adelmann1, Nancy Heylen1, Geraldine Jamieson1, Jeffrey Smith2, Angélique, Raley2, Anton deVilliers2, Serge Biesemans2, Christopher J. Wilson1, Gert Leusink2 and Zsolt Tőkei1
1imec vzw, Kapeldreef 75, B-3001, Leuven, Belgium. 2TEL Technology Center, America, LLC, Albany, NY, USA

High-aspect-ratio (HAR) Ru buried power rail (BPR), can potentially replace conventional back-end-of-line (BEOL) Cu power rails. One of the key steps of BPR integration is the metal recess etch, necessary for its electrical isolation with overlying gate and enables metal encapsulation, necessary for contamination control during downstream front-end-of-line (FEOL) processing. This paper demonstrates controlled recess of ~50 nm of Ru metal - TiN liner in lines of AR~8, CD~15 nm. Recessed line resistance measures at 91 Ω/μm with a 3σ of 30 Ω/μm across the wafer. For the recessed line, an electrical resistivity of 10.3 μΩcm is extracted from the temperature-controlled-resistance (TCR) measurements.

4.09. A Novel Airgap Formation Scheme by Coating Process123456789
Xiaoxu kang *, Ruoxi Shen, Xiaolan Zhong, Shoumian Chen, Yuhang Zhao
Process Technologies Department Shanghai IC R&D Center, ICRD Shanghai, China

With CMOS technology developing, interconnect RC delay is becoming more and more important to the chip performance, and driving more and more needs for new materials and approaches into CMOS BEOL integration. Introduction of low-k material can reduce the parasitic capacitance, and airgap is the ultimate low-k material with the lowest dielectric constant close to 1. Normally airgap was formed by sacrificial layer release or non-conformal CVD dielectric deposition, which will increase the process complexity and cost. In this work, a new scheme was proposed to form the airgap by low-cost coating process in which Graphene Oxide (GO) sheet was used as gap-filling suppressor to seal the gap between two adjacent metal line and form the airgap. Patterned metal line with larger space and fork structure was fabricated to form the gap and evaluate the process performance. For the gap region, volume ratio of GO sealed airgap to gap region before sealed can reach to about 85% and calculated effective relative dielectric constant of this region is about 1.57.

4.10. Vapor Phase Thiol Self-Assembled Monolayers Enabling Area Selective Deposition.
Sebastiaan J. F. Herregods, Tinne Delande, Zsolt Tokei, Herbert Struyf, Silvia Armini
Imec Leuven, Belgium

Area Selective deposition (ASD) gained great interest due to its possible application in bottom-up self-aligned schemes. Vapor phase n-undecanethiol (UDT) depositions on oxidized copper led to multilayer formation passivating the surface against HfNx Atomic Layer Deposition (ALD). The selectivity was investigated on blankets and nanopatterned Cu/SiO2 structures with variable pitch by RBS, TDSEM and AFM. Selective deposition of up to 8.8 nm HfNx on SiO2/Cu lines exhibited

undesired passivation at the edge of the SiO2 growth surface and high line edge roughness of the ASD HfNx layer. This issues was mitigated by better confining the UDT film to the Cu lines by performing a forming gas treatment prior to the ALD.

4.11. Highly conformal, low resistance ruthenium deposited from p-cymene-1,3-cyclohexadiene ruthenium

Philip Chen, Eric Condo, Susan DiMeo, Bryan Hendrix, Thomas Baum
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PEALD and thermal CVD with p-cymene-1,3-cyclohexadiene ruthenium (p-Cymene CHD Ru) precursor were used to deposit Ru thin films on TiN and thermal oxide substrates using NH3, O2, and H2 as co-reactants. The growth rate, film resistivity, and surface morphology of deposited Ru thin-films were compared for the various processes. Resistivity <100μΩ-cm is demonstrated at 15Å thickness; PEALD and CVD processes can provide 30μΩ-cm in the 40-60Å range. Roughly 70% step coverage of Ru deposition was demonstrated on a trench structure with aspect ratio of ~25 using the CVD process.

4.12. Slurry design for robust planarization of low k organosilicate glass films

*Anupama Mallikarjunan, *Rung-Je Yang, *Chen-Yuan Huang, *Shih-Hsuan Chao, *Ming-Shih Tsai, and *Chris Li
Jennifer Achtyl, Lu Gan, Dnyanesh Tamboli, Robert Ridgeway, James Schlueter, and Mark O'Neill
**Asia Technology Center for Planarization Versum Materials, Zhudong Township, Taiwan*
Advanced Deposition Materials and Planarization Technology Versum Materials, Tempe, AZ, USA

Low κ Organosilicate Glass (OSG) films are being proliferated into new IC device architectures with a wide range of CMP requirements (highly selective to non-selective polishes, low polish rates to high polish rates). In this paper, the relationship between OSG film properties (both bulk and surface) and their planarization response, especially removal rate (RR) was first characterized. Eight OSG films were polished using advanced barrier slurries. The films ranged in carbon content from 8 to 24 % and in nanoindentation elastic modulus from 5.5 to 21.8 GPa. An inverse relationship was observed between RR and the bulk chemical bonding structure (Si(CH3)x/SiOx peak area ratio as determined by transmission infrared spectroscopy measurements). In addition, the OSG film's surface free energy post-polish (measured from water and diiodomethane contact angles) varied systematically only with the film's Si(CH3)x/SiOx ratio. Based on the above learning, a new slurry was formulated and planarized all the OSG films at a similar rate. Such a slurry is better suited for robust manufacturing, as removal will not be affected by differences in OSG film composition.

4.13. Thermal stability and permeability of ultrathin Ta(N) barrier in Cu interconnect

Zheng-Jun Hu1,2,°, Haoyu Xu3°, Xin-Ping Qu1*, Hao Wan2, Shen-Suo Yan2, Ming Li2, Shou-Mian Chen2, Yu-Hang Zhao2, Jing Zhang3 and Mikhail R. Baklanov3
1. State key lab of ASIC and system, School of microelectronics, Fudan University, Shanghai 200433, China
2. Shanghai IC R&D Center, Shanghai 201210, China
3. North China University of Technology, Beijing, China

The thermal stability and barrier integrity of ultrathin Ta(N) barrier (1-3 nm) for Cu/low k (k=2.55) interconnect have been investigated. It is shown that though the system with TaN (2s) has best thermal stability, yet the permeability of Ta(1s)/TaN(1s) structure is slightly less than that of TaN(2s) on low k. Results show that the 2 nm thick barriers have sufficiently good barrier properties, while 1 nm thick films are permeable for water and solvent molecules.

4.14. Temperature-Dependent Resistivity of Alternative Metal Thin Films

Marco Siniscalchi,1,2 Davide Tierno,1 Sofie Mertens,1 Christopher J. Wilson,1 Zsolt Tőkei,1 Sven Van Elshocht,1 and Christoph Adelmann1
1Imec, 3001 Leuven, Belgium - 2Dipartimento di Chimica, Materiali e Ingegneria Chimica, Politecnico di Milano, 20131 Milano, Italy

The temperature coefficient of resistivity (TCR) has been measured for Cu, Ru, Co, and Ir thin films

with thicknesses down to 3 nm to assess the dominant electron scattering mecha-nism in these films. Ru, Co, and Ir show bulk-like TCR values down to 5 nm with some signs of disorder-induced TCR lowering for 3 nm for Ru and Co. By contrast, Cu shows a considerably larger TCR value than bulk that increases with decreasing thick-ness. The results are qualitatively consistent with calculations of the TCR within a semiclassical model.

4.15. Study of Cobalt Wet Recess for Fully Self Aligned Vias in Advanced Interconnects
Yuya Akanishi, *Antoine Pacco, *Frank Holsteyns
*SCREEN Semiconductor Solutions Co., Ltd. Hikone, Japan, *imec Kapeldreef 75, 3001 Leuven, Belgium*

Controlled wet recess process of Co combined with TiN barrier removal is demonstrated. By applying sequential repetition process of wet oxidation and oxide removal step, it is confirmed that the Co is successfully recessed with good controllability by the number of repetition cycles. TiN removal is also demonstrated with post hot APM.

4.16. Comparative Study on Atomic Layer Deposited Ru and Pt as an Interconnect Material to Replace Cu
Seung-Min Han, Yong-Hwan Joo, Dip K. Nandi, Soo-Hyun Kim
School of Materials Science and Engineering, Yeungnam University 214- 1, Dae-dong, Gyeongsan-City, South Korea, 712-749

Ruthenium (Ru) and platinum (Pt) thin films were deposited on SiO2 (100nm)/Si substrates using novel metal-organic precursors and diluted O2 as reactant at the temperature ranging from 200 °C to 225 °C. Both ALD processes revealed linear growth with the number of ALD cycles with a very short (~7cycles) incubation (for Ru) or without any incubation period (for Pt). The resistivity of as-deposited ALD-Ru (25 nm in thickness) is considerably low (~24 μΩ-cm) at optimized deposition condition and could be further reduced to 16.57 μΩ-cm upon annealing at 400 °C. Interestingly, the resistivity of as-deposited ALD-Pt is as low as ~12.8 μΩ-cm (40 nm in thickness) which is almost same as its bulk resistivity (10.6 μΩ-cm) and kept its low value of 18 μΩ-cm even to 10 nm.

4.17. MoCl5 Intercalation for CVD Graphene at Low Temperature using High Chemical Concentration
Ekkaphop Ketsombun*, Kosuke Yokosawa*, Kazuyoshi Uenoa,*1 Xiangyu Wua,b, Inge Asselberghs-b, Swati Achra-a,b, Cedric Huyghebaert-b, and Zsolt Tokei-b
**Grad. School of Eng.Sci., *1Res. Cen. for Green Innov., Shibaura Institute of Technology, Tokyo, Japan ueno@shibaura-it.ac.jp*
a KU Leuven, 3001 Leuven, Belgium, b imec, Kapeldreef 75, 3001 Leuven, Belgium

Efficient doping method is required to reduce the resistance of graphene interconnects. This paper proposes a MoCl5 intercalation process for doping CVD graphene at a low-temperature of 150 ºC using high concentration of MoCl5 chemicals. Bilayer graphene (BLG) was successfully doped at 150 ºC without serious damages within a short process time as 30-60 min. The uniformity of doping was improved by increasing the reaction time.

4.19. Molybdenum as an Alternative Metal: Thin Film Properties
V. Founta,1,2 T. Witters,1 S. Mertens,1 K. Vanstreels,1 J. Meersschaut,1 P. Van Marcke,1 M. Korytov,1 A. Franquet,1 C. J. Wilson,1 Z. Tőkei,1 S. Van Elshocht,1 and C. Adelmann1
1 Imec, 3001 Leuven, Belgium, 2 Department of Materials Engineering, KU Leuven, 3001 Leuven, Belgium

The structural and electrical properties of Mo thin films have been studied to assess the potential of Mo as an alternative to Cu or W metallization. The adhesion energy with dense low-κ dielectrics was above 5 J/m2, suggesting that Mo can be integrated without the need for an adhesion liner. The Mo resistivity was lower than W in the entire thickness range between 3 and 50 nm and lower than Cu sandwiched between 1.5 nm TaN barriers for total a stack thickness below 8 nm. Mo thus appears promising as an interconnect metal, especially a potential replacement for W.

4.20. Graphene-Ruthenium hybrid interconnects
Swati Achra1,2, Inge Asselberghs2, Xiangyu Wu1,2, Steven Brems2, Cedric Huyghebaert2, Bart Sorée1,2, Marc Heyns1,2 and Zsolt Tokei2
1 KU Leuven, 3001 Leuven, Belgium, 2 imec, Kapeldreef 75, 3001 Leuven, Belgium

We propose a potential integration of few-layer graphene (FLG) in interconnects with Pt-group transition metals, such as Ruthenium (Ru). We demonstrate graphene/Ruthenium (G/Ru) hybrid structures realized by transferring graphene onto Ru thin film. Graphene is shown to adhere well to large area Ru where Raman spectra shows the impact of metal induced charge doping for single, bilayer and fewlayer graphene on 5nm thick Ru film. We measure a drop of 15% in electrical resistivity of Ru when encapsulated with graphene. Temperature coefficient of Resistance (TCR) of G/Ru hybrid wires is reduced by a factor of 1.7 as compared to Ru wires. Thus, our findings establish a possible route for hybrid carbon/metal interconnects.

4.21. Electrical Characterization of MoCl5 Intercalated Graphene Interconnects
Xiangyu Wu1,2,*, Inge Asselberghs2, Ekkaphop Ketsombun3, Kosuke Yokosawa3, Swati Achra1,2, Steven Brems2, Cedric Huyghebaert2, Marc Heyns1,2,Bart Sorée1,2, Kazuyoshi Ueno3 and Zsolt Tokei2
1 KU Leuven, 3001 Leuven, Belgium, 2 imec, Kapeldreef 75, 3001 Leuven, Belgium, 3 Shibaura Institute of Technology, 3-7-5 Toyosu, Koto, Tokyo 135-8548, Japan

In this work, we study the influence of MoCl5 intercalation on the electrical performance of graphene interconnects. It is found that intercalation doping can effectively reduce the sheet resistance by increasing carrier concentration. Resistivity of 30 μΩcm and 14 μΩcm is reached for the AB-stacked BLG (AB-BLG) and twisted BLG (t-BLG), respectively.

4.22. CoxMoy alloy as a single layer barrier for Co interconnect
Tong Teng and Xin-Ping Qu*
State key lab of ASIC and system, Fudan University, Shanghai 200433, CHINA

Oxygen barrier, adhesion and BTS-CV properties of a single diffusion barrier CoxMoy for cobalt interconnect has been investigated. Results show that, the anti-oxidation property, adhesion with SiO2, and Bias-temperature CV flatband shit of the Co1Mo3 barrier is better.

4.23. A New Cu(NbCNx) Film and its Characteristics
Chon-Hsin Lin*
**Center for Generation Education, Asia-Pacific Institute of Creativity, Toufen, Miaoli 351,Taiwan*

In this study, a new barrierless Cu(NbCNx) copper (Cu) alloy film is created using barrierless Cu metallization with two types of thickness by co-sputtering copper, niobium (Nb) and carbon (C) on silicon (Si) substrates within either an Ar or an Ar/N2 vacuum charmer having a pressure of 10-4 Torr. Various composition sets were explored in search of an optimal composition for the new film to exhibit a lowest resistivity-- a vital indication of good conductivity for the film's possible interconnect use in the microelectronics industry, which is the main goal of the study. The resistivity values of 300 nm- and 8 nm-thick pure Cu, Cu(NbC) and Cu(NbCNX) films after isothermally and cyclically annealing at various temperatures were respectively measured and presented herein. The cross-sectional TEM image of the Cu(NbCNx) film after annealing is shown, and a 2.56Å d-spacing of NbCNx phase solidly dissolved in the Cu(NbCNx) film is observed. The XRD patterns of an Sn/Cu(NbCNx)/Si structure as-deposited and after an 8-day aging were analyzed, which reveals that the stability improvement of the new film seems to be caused by the NbCNx formed within Cu(NbCNx). The TDDB lifetime vs. electric strength curves of the three films mentioned show that the new film meets the 10-year projected reliability up to 1MV/cm, making the new film a promising candidate material for circuit-printing conductors and copper interconnects in microelectronic applications.

4.24. The resistivity and electrical stability of Ni silicide nanowire formed on SOI
Gang-qiang Shu, Tong Teng, Xinhui Qin and Xin-Ping Qu
State key lab of ASIC and system, Fudan University, Shanghai 200433, CHINA

In this work we fabricated Ni silicide nanowires by using electronbeam lithography and reactive ion etching process, which is a subtractive method. Our work shows that low resistivity (10~20 μΩ·cm) of NiSi nanowire with width from 100 nm to 40 nm can be obtained. The silicide nanowire can withstand very high current density at 1.5E7A/cm2 for 5100 s.

4.25. Reduction of Ni(Pt)SiGe/SiGe Contact Resistivity either by Ge Pre-amorphization Implantation (PAI) or Si Capping and Comparision between Both

Shujuan Mao, Guilei Wang, Jing Xu, Dan Zhang, Xue Luo, Wenwu Wang, Dapeng Chen, Junfeng Li, Chao Zhao, Tianchun Ye, Jun Luo
Key Laboratory of Microelectronic Devices & Integrated Technology Institute of Microelectronics, Chinese Academy of Sciences Beijing, China

This work investigates the contact resistivity (ρc) of Ni(Pt)SiGe/SiGe with Ge PAI and Si capping process respectively. It is found that ρc of Ni(Pt)SiGe/SiGe is reduced remarkably either by using Ge implantation to amorphize SiGe before germanosicidation or employing an epitaxial Si-cap layer on SiGe. Comparatively, Si capping process is somewhat superior to Ge PAI process with a lower ρc of 1.44×10-8 Ω-cm2 obtained.

4.26. New Insight on Surface Preparation Impact on Co Silicide Formation

M.Gregoire, E. Ghegin, K. Dabertrand, A.Valery, M. Juhel, and L.Esposito.
Silicon Technology Development STMicroelectronics Crolles France

In the frame of advanced imager and flash memories technologies development, Co silicide resistivity, roughness, Si penetration, and thermal stability need to be improved to meet technologies requirements. For Ni-based silicide, the optimization of the surface preparation process leads to suitable changes in the silicide formation. In this paper, we investigate the influence of two different surface preparation processes, i.e. Ar sputter etch and Siconi pre-clean, on Co silicide properties. At the end, Siconi pre-clean reduces the Co silicide resistivity by 14% by limiting the O contamination inside the silicide layer, and modifying the final CoSi2 layer microstructure.

4.27. Integration of Carbon Nanotube as Via Contact to MoS2

Zichao Ma, Ying Xiao, Clarissa Prawoto, Zubair Ahmed, Mansun Chan, *Changjian Zhou
Department of Electronic & Computer Engineering Hong Kong University of Science and Technology Hong Kong
**School of Electronic and Information Engineering South China University of Technology Guangzhou, China*

This paper demonstrates direct growth of carbon nanotubes on MoS2 layers for the first time, to achieve via interconnect that can carry current density over 107 A/cm2. CNT growth on the pristine MoS2 layers is achieved by specially designed Ti-Ni dual-metal catalyst. The growth temperature is limited to 550℃ as high temperature causes damage to MoS2 lattice. The series resistance from metal-CNT to the MoS2 film is measured to be 4 MΩ·μm.

4.28. WS2 MOSFETs: Significant Performance Improvement with Mg Contacts

Surajit Sutar, Massimo Mongillo, Salim El Kazzi, Inge Asselberghs, Cedric Huyghebaert, Matty Caymax, Dennis Lin, and Iuliana Radu
IMEC Heverlee, Belgium

Exploration of metals with < 4 eV or >5 eV work function as contacts to WS2 shows predominantly n-type conduction in exfoliated and CVD-grown WS2. Of the set, Mg contacts show the best n-MOSFET performance with ≈200 μA/μm current density without any special substrates or processing techniques, enabling reliable estimates of the intrinsic mobility from techniques such as TLM, 4-probe, and Hall measurements. The results from all three techniques are observed to be consistent with each other, showing >100 cm2/s electron mobilities at room temperature.

4.29. Al and TiN Gate Electrodes for Vertical MOS and Tunnel FETs in the Same Silicon Pillar Structure

Luís Francisco Pinotti, José A. Diniz, Frederico H. Cioldin*, Alfredo R. Vaz*, Luana C.J. Espinola*
*FEEC (Faculdade de Engenharia Eletrica e de Computacao) Unicamp Campinas, Brazil, *CCSNano Unicamp Campinas, Brazil*

As an innovation, this work presents a silicon pillar structure containing both MOS (Metal-Oxide-Semiconductor) and Tunnel Field Effect Transistors (MOSFETs and TFETs, respectively) with double gates (with Al or TiN metal gate electrodes). The abrupt n+ regions of drain/source in the p-Si vertical pillar are obtained from sequential 31P+ ion implantations (energies of 100, 50 and 25keV) and Rapid Thermal Annealing (RTA). The abrupt drain region in the p-Si pillar allows the vertical control of the channel length of the MOSFET device (achieving lengths such as 70nm) and the formation of a nano intrinsic region (2nm), between n+ and p regions, fundamental for the operation of a TFET. The MOSFETs and TFETs, which were fabricated with Al gate, have presented the better results (Ion of 1mA, gm of 900µS and (Ion/Ioff) ratio of 107) related to higher performance in conduction regime. However, both devices, fabricated with TiN, have presented higher performance related to leakage and/or off current (Ioff of 36pA).

4.31. A Thin Bonding Material for High Density Device Stacking

Yasuhisa Kayaba, Yuzo Nakamura, Jun Kamada, and Kazuo Kohmura
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A new thin bonding material is developed for the 3D device stacking by Cu-Cu hybrid bonding. The bonding material is bondable to SiO2, Si3N4, SiCN at room temperature, and it has 400˚C thermal stability. By using this bonding material, wafer or chip are bondable with no thermal sliding in micrometer range. Cu-Cu hybrid bonding with no void is also shown.

4.32. Blister-free thermal atomic layer deposition of ruthenium with an additional hydrogen purge

Sebastian Killge, Nils Alexander Hampel, Marcel Junige, Johanna Reif, Volker Neumann, Martin Knaut, Christian Wenzel, Matthias Albert, Johann W. Bartha
Technische Universität Dresden, Institute of Semiconductor and Microsystems (IHM) Dresden, Germany

This paper presents a novel blister free thermal activated atomic layer deposition (thALD) of ruthenium (Ru) seed in high aspect ratio through silicon vias (HAR-TSVs) for application in next-generation integrated circuits. ThALD of ruthenium (5 - 12 nm thick) for seed layer preparation was carried out by reaction of the organometallic precursor ECPR [(ethylcyclopentadienyl)(pyrrolyl) ruthenium(II)] with molecular oxygen on a TaN barrier deposited by thermal ALD of (tert-butylimido)tris (diethylamino) tantalum(V) (TBTDET) and ammonia (NH3) as co-reactant. Major problems of such ALD grown ruthenium turned out to be a weak layer adhesion on tantalum nitride and a special type of undesired delamination called blister formation negatively affecting the reliability of layers and subsequent electrochemical deposition of copper. Both effects can be fully prevented by additional purge steps with hydrogen during ALD. In order to clarify this, we investigated the Ru-ALD nucleation in detail. Additionally, the impact of the deposition temperature between 200 and 250 °C was studied.

4.33. RF Characterization and Design of Multi-TSV with Embedded Capacitor

Neeraj Panwar1,*, Anak Agung Alit Apriyana1, 2, Ye Lin1, and Chuan Seng Tan1,*
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This paper presents RF characterization and design of multi-TSV with embedded capacitor up to 10GHz. The capacitor is embedded around the TSV structure prior to Cu filling to utilize the vertical dimension, and thus improves the capacitance density and silicon area utilization. Here, the

capacitance response with respect to variations in structural dimension such as TSV height, diameter, metallization and dielectric thickness are systematically studied. The results show that the increase in the thickness of Cu (electrode metal) continuously improves the Q-factor without any significant degradation in capacitance, which enables these capacitors to be used at higher frequency. Also, the thickness of TiN (used as diffusion barrier layer on both side of Cu electrode) neither affects the Q-factor nor the capacitance.

4.34. UBM and solder metallurgy selection for fine pitch 3D stacking
Jaber Derakhshandeh, Lin Hou, Inge De Preter, Carine Gerets, Kenneth June Rebibis, Andy Miller, Gerald Beyer and Eric Beyne
Imec, 3D system and technology group Leuven, Belgium

In this paper we present a complete study on the properties of different metallurgy systems in terms of IMC growth rate at different temperatures and times, IMC surface morphology and voiding. After theoretical calculations for UBM consumptions and volume shrinkage, IMC growth parameters such as activation energy and interdiffusion coefficients for Cu/Sn, Ni/Sn and Co/Sn systems will be shown.

4.35. Low-Viscosity Underfill Technology with Negative-CTE Filler for High-Density 3D Interconnections
Hisashi Kino1 Takafumi Fukushima2, and Tetsu Tanaka2,3
1. Frontier Research Institute for Interdisciplinary Sciences (FRIS), Tohoku University Sendai, Japan
2. Graduate School of Engineering,3. Graduate School of Biomedical Engineering, Tohoku University Sendai, Japan

Several stacked chips in 3D ICs are electrically and mechanically interconnected by metal microbumps and underfill material. The underfill material is injected between the metal microbumps by capillary forces. Thus, a low-viscosity underfill material is strongly required to achieve a high-density metal microbump interconnection with void-free underfilling. In general, the underfill consists of an epoxy and microparticles called filler, which can reduce the coefficient of thermal expansion (CTE) of the underfill. Then, to reduce the CTE of the underfill, high-concentration filler is also required. However, high-concentration filler induces an increase in the viscosity of the underfill. In this study, we proposed an underfill with a negative CTE filler, which can reduce the CTE of the underfill at a lower concentration compared with conventional filler. This paper reports the effect of negative-CTE filler on the mechanical and electrical characteristics of the underfill

4.36. Room Temperature SiO2 Liner Technology for Multichip-to-Wafer 3D Integration with Via-last TSV
Rui Liang1, Sungho Lee2, Yuki Miwa1, Hisashi Kino3, Takafumi Fukushima2, and Tetsu Tanaka1,2
Graduate School of Biomedical Engineering1, Tohoku Univ. Sendai, Japan
Graduate School of Engineering2, Frontier Research Institute for Interdisciplinary Sciences3, Tohoku Univ. Sendai, Japan

Through-silicon vias (TSVs) is one of the most important technologies in 3D integration. In order to form a high-quality and conformal insulation layer on the sidewall of TSVs in the via-last/backside-via process, a high-temperature process is usually required. However, the high temperature process gives negative effects on temporary adhesives, which is usually used for adhesion between the IC chips/wafer and the support wafer. This trade-off causes several issues and challenges. In this study, we applied OER (Ozone-Ethylene Radical generation) TEOS-CVD method to TSV dielectric liner formation for the first time. We also evaluated dielectric liner characteristics with TSV-structured metal-insulator-semiconductor (MIS) capacitor for multichip-to-wafer (MC2W) 3D integration process. The OER-TEOS-CVD SiO2 liners were compared to that formed by conventional PE-CVD. We confirmed significant hysteresis suppression of the C-V curve with the MIS capacitor formed by room-temperature (RT) OER-TEOS-CVD. The SiO2 liner formed by RT-OER-TEOS-CVD also showed an excellent step coverage on the sidewall of the deep-via hole. These results indicated that RT-OER-TEOS-CVD was a potential candidate to fabricate reliable TSV liner in the 3D integration process.

4.37. Design of a Long-Distance Quantum Interconnect for Spin Qubits using Superconducting Resonators

F. A. Mohiyaddin1,3, N. I. Dumoulin Stuyck2,3, B. Govoreanu3, R. Li3, A. Potočnik3, J. Verjauw2,3, F. Ciubotaru3, S. Brebels3, B. T. Chan3, J. Jussot3, S. Kubicek3, A. Spessot3, I. P. Radu3
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Long-distance interconnects are a pre-requisite for building a large-scale quantum processor. In this paper, we report the design of a quantum interconnect for silicon quantum bits (qubits) with superconducting microwave resonators. We elaborate on the appropriate geometry, critical dimensions and materials for the interconnect, based on several multi-physics models. We finally estimate coupling strengths that are achievable between qubits via the interconnect.

4.38. Beyond BEOL Interconnect Wafer Level Monolithic Near-Infrared/Infrared Thin Film Photo Diode Image Sensor Integration

Yunlong Li, David Cheyns, Luis Moreno Hagelsieb, Epimitheas Georgitzikis, Myung-Jin Lim, Ming Mao, Thomas Witters, Kenny Leyssens, Pierre Boulenc, Jiwon Lee, Pawel E. Malinowski, Stefano Guerrieri
Imec, Kapeldreef 75, B-3001 Leuven, Belgium

Processing thin film photo-diode based image sensor at wafer level is promising for near-infrared and infrared image sensing applications as automotive and consumer electronics. However, there are lots of challenges to do wafer level process with pure organic or organic matrix based thin films which behaves significantly different than Si. To achieve a high yield for thin film photo-diode based pixel array with millions of pixels, the defectivity needs to be as low as possible. In this paper, we discuss the process modules and development status for PbS quantum dots and organic polymer based thin film photo-diode prototype at imec.

17:30 – 20:00
Lam Research Technology Networking Session - Royal A and B rooms, 1st floor
Lam Research invites you to join us for an evening reception and technology seminar on “Addressing Interconnect Challenges”. Come hear talks by industry experts from imec and Leti as they share their perspectives on advanced interconnect and packaging developments. Light hors d’oeuvres and refreshments will be served.

TECHNICAL PROGRAM: WEDNESDAY 5TH JUNE

Session 5 - Memory Integration

Royal A and B rooms, 1st floor
Session Chairs: Christophe Detavernier, *University of Gent*, Nicola Nastasi, *Micron*

08:15 - 08:45
5.1. INVITED - 3D Flash Memory Technology, BiCS FLASHTM
Masayoshi Tagami, *Toshiba Memory*

Due to the advent of the Internet of Things (IoT), the prevalence of social networking services (SNSs), and production of photos and videos at ever-higher resolution, the volume of data generated worldwide is growing exponentially. In the field of information processing, real-time performance is considered an important requirement as a huge amount of data must be managed by big-data systems or indefinitely stored by data centers and cloud service systems. In this situation, high-capacity storage is required to process, store and manage large quantities of data at high speed and low power consumption. Furthermore, for smartphone, tablet, memory card and other power-sensitive applications, demand for storage with lower power consumption is increasing.

BiCS FLASHTM, which offers many advantages over planar NAND flash memory, will be the solution satisfying the market requirements. The vertically stacked threedimensional (3D) flash memory, BiCS FLASHTM, has far higher die area density compared to the prior state-of-theart technology, two-dimensional (2D) NAND flash memory. Moreover, BiCS FLASHTM reduced the chip size by optimizing both circuit technology and manufacturing process. In this paper, the concept and technologies for BiCS FLASHTM will be presented.

08:45 - 09:15
5.2. INVITED - Interconnects for Tera-byte 3D Application
Takayuki Ohba, *Tokyo Institute of Technology*

The prospect of three-dimensional (3D) integration for Terabyte large scale integration using bumpless interconnects with low-aspect-ratio TSVs and ultra-thinning are discussed. Bumpless (no bump) interconnects between wafers are a second-generation alternative to the use of micro-bumps for Wafer-on-Wafer (WOW) technology. Ultra-thinning of wafers down to 4μm provides the advantage of a small form factor, not only in terms of the total volume of 3D ICs, but also the aspect ratio of Through-Silicon-Vias (TSVs). The bumpless interconnects technology can increase the number of TSVs per chip with a finer pitch of TSVs and lower the impedance of the TSV interconnects with no bumps. Therefore, a promising operating platform with a higher speed by enhancing parallelism, lower power by no bumps, and smaller size by thinning wafers can realize.

09:15 - 09:40
5.3. Indium Tin Oxide Electrode for Highly Reliable (Pb,La)(Zr,Ti)O3 Capacitors through D2 Exposure
Atsushi Kobayashi, Yoko Takada, Naoki Okamoto, Takeyasu Saito, *Rie Shishido, °Koji Higuchi, °Akira Kitajima
*Dept. of Chemical Engineering Osaka Prefecture University Sakai, Japan, *Institute of Multidisciplinary Research for Advanced Materials Tohoku University Sendai, Japan °The Institute of Scientific and Industrial Research Osaka University Ibaraki, Japan*

Ferroelectric random-access memory (FeRAM) is one of the promising candidates for future nonvolatile memory devices. High density FeRAM requires more robust electrode material for capacitor reliability to replace Pt or Ir electrodes. In this study, pulsed laser deposited (PLD) or DC sputtered Sn-doped In2O3 (ITO) was employed for bottom and top electrodes of (Pb,La)(Zr,Ti)O3 (PLZT) capacitor. The ferroelectric properties of PLZT capacitors with ITO electrodes by PLD and sputtering were successfully obtained as ca. 50 μC/cm2 and 60 μC/cm2, respectively. It was also found that degradation characteristics were much stable and ITO plays a role as D2 barrier after 120 minutes D2 exposure at 200°C.

09:40 - 10:05
5.4. Advanced TEM-based Characterizations For Bits Fail Analysis In 28 nm Phase Change Memory Test Vehicle
A. Valery, K. Dabertrand, R. Bon, L. Clément
STMicroelectronics Crolles, France

Combining multiple transmission electron microscopy-based techniques is essential to investigate the material properties in Phase Change Memory cells. Physical characterizations of failing bits are powerful solutions to support technology development: the analysis of chalcogenide material properties and its evolution can very effectively help to optimize several integration steps. In this study, a first example reveals a local change of the material crystalline state is at the origin of Reset bit fails without altering the spatial distribution of elements in the layer. A second example focused on Set bit fails shows Ge clusters made of several grains can be considered at the origin of degraded cell reading current.

10:05 - 10:25
AM Break

Session 6 - Dielectrics
Royal A and B rooms, 1st floor
Session Chairs: Takahiro Kouno, *Socionext*, Fabrice Nemouchi, *CEA-Leti*

10:25 - 10:55
6.1. INVITED - Robust ULK engineering for performance and reliability
Sang-Hoon Ahn, *Samsung Electronics*

UV-based low-k recovery process was developed at post etch/strip step to reduce Cu/ULK (ultralow-k) interconnect capacitance by 3.0% and 4.0% at 32nm and 24nm wide line, respectively. TDDB lifetime was also improved by 5 orders of magnitude by power law model at 32nm wide line. In addition to low k damage recovery effect, the recovery process was found to be capable of indirectly contributing to EM improvement by a factor of three over the reference. In fact, TEM EDX confirmed that the recovery process induces more Manganese to migrate from alloy seed to the interface between Cu and dielectric barrier. Its ULK surface densification and smoothening effects seemingly pave a way for continuous and dense TaN/Ta barrier liner formation together with a lower level of moisture and fluorine within the damage-recovered low k IMD. Finally, the reducing treatment prior to the recovery process eliminates the surface Cu oxide that works as possible reaction sites for the recovery chemical, thus suppressing via resistance increase.

10:55 - 11:20
6.2. Robust Low k C-rich SiCN Interlevel Dielectric with Ultrathin Barrier for Novel RC Reduction in BEOL Cu-Low K SiCN Interconnects
Son Van Nguyen1, H. Shobha1, T. Haigh1, J. Chen1, J. Lee1, T. Nogami1, E. Liniger2. S. Cohen2, C. K. Hu2, H. Huang1, Y. Yao3, D. Canaperi1, B. Peethala1, T. Standaert1 and G. Bonilla2.
1 IBM Semiconductor Technology Research, Albany, NY 12203 USA, 2 IBM T.J. Watson Research Center, Yorktown Heights, NY, 10598 USA, 3 IBM STG Hopewell Junction, NY, 12533 USA

Mechanically robust low k C-rich SiCN and pSiCN dielectrics with excellent built-in Cu oxidation and diffusion barrier have been developed and evaluated as potential alternative low k Interlevel dielectrics for Cu interconnects. The novel low k dense C-Rich SiCN (k=3.3) and lightly porous C-Rich SiCN (k=2.8) films have high modulus (E~> 15-30 GPa) and significantly lower Plasma Induced Damage (PID) as compared to typical pSiCOH (k~2.4-2.7) dielectrics. The excellent Cu diffusion barrier properties of these SiCN dielectrics enable the use of thinner metallic Cu barriers that resulting in larger Cu line's volume, reduced resistance and overall RC in sub-50 nm pitch interconnects without TDDB and EM reliability penalty. The high modulus dielectrics also enable high aspect ratio sub-40 nm patterning without pattern collapse.

11:20 - 11:45

6.3. Down scaling area-selective deposition to sub-30 nm half-pitch lines
Mattia Pasquali, Stefan De Gendt, Gayle Murdoch*, Zsolt Tokei*, Silvia Armini*
*Department of Chemistry, Faculty of Science KU Leuven, Leuven, Belgium. S*emiconductor Technology and Systems IMEC, Leuven, Belgium*

Self-Aligned patterning schemes, such as Area Selective Deposition (ASD), are getting increasing attention due to current challenges caused by ever-shrinking features' critical dimensions. ASD can be achieved by exploiting surface-sensitive technique like Atomic Layer Deposition (ALD). However, ALD inherent selectivity is confined to very few ALD cycles. Self-Assembled Monolayers (SAMs) are evaluated as a metal passivation coating to extend the ASD process window. We present a successful strategy to achieve selective deposition of Al oxide on Cu/SiO2 patterned substrate down to sub-30nm half-pitch (HP) lines. We exploit the selective chemisorption of Octadecylthiol on Cu over SiO2 to prevent Al oxide ALD on the former material. ASD up to 6nm is demonstrated at relevant nano-scale dimensions with Al on Cu below EDX detection limits.

11:45 - 12:10
6.4. Ion Implantation and Laser Annealing for Toughening Low-k Dielectric in Scaled-down Interconnects
D. Sil, O. Gluschenkov, Y. Sulehria, D. Durrant, H.Huang, N. Lanzillo, H. Shobha, N. O'Haller, Y. Yao, M. Sunder, C. R. Thomas, J. Lee, M. Shoudy, S. Nguyen, T. Nogami, C. B. Peethala, B. Haran, J. Liu*, S. Halty,* and F. Mazzamuto*
*IBM Research, Albany, USA, *Screen LASSE, Albany, USA*

A low-dose ion implantation and/or nanosecond laser annealing were employed to significantly strengthen porous low-k films with a limited impact on its k. Toughened high-porosity ILD films exhibited a significant increase in PID resistance and a dramatic rise in TDDB lifetime at equivalent k or enabled a robust BEOL integration at a lower RC delay point demonstrating 6-12% RC delay reduction over the present ILD baseline (k ~ 2.77).

12:10 - 13:25
Lunch

Session 7 - Contacts I
Royal A and B rooms, 1st floor
Session Chairs: Luke Henderson, *BASF*, Mehul Naik, *AMAT*

13:25 - 13:55
7.1 INVITED - Understanding and control of Fermi level pinning at metal/germanium interface
Tomonori Nishimura, *University of Tokyo*

This paper discusses the strong Fermi-level pinning (FLP) at metal/germanium (Ge) interface. From a relationship of FLP strength among Si, SiGe and Ge, and from an impact of ultrathin insulator insertion on the FLP, it seems reasonable that the FLP is dominantly caused by intrinsic metal-induced gap states (MIGS) which is described as wave function tailing. We also reconsider MIGS from metal side and demonstrate FLP alleviation at direct metal/Ge interface. It is a key to realizing practical metal/Ge contact with low resistance in Ge devices.

13:55 - 14:20
7.2. Challenges of Contact Scaling and Opportunities of Co/CoTix
Maryamsadat Hosseini1* and Junichi Koike2
1 Department of Solid State Sciences, Ghent University, Ghent, Belgium, 2 Department of Materials Science, Tohoku University, Sendai, Japan

A new amorphous alloy of CoTix is proposed to provide all required functions of liner, diffusion barrier, and low resistive contact for a plug structure on p and n+-Si. A low specific contact resistivity and Schottky barrier height can be obtained with reaction between CoTix and Si.

14:20 - 14:45
7.3. Towards the integration of Ni/InP contact module in 300 mm
F. Boyer∗†‡, P. Gergaud†, D. Mariolle†, N. Chevalier†, K. Dabertrand∗, S. Favier∗, N. Coudurier†, F. Nemouchi†, M. Gr´egoire∗, Q. Rafhay‡ and Ph. Rodriguez† *∗STMicroelectronics, 850 rue Jean Monnet, BP 16, 38926 Crolles, France, †Univ. Grenoble Alpes, CEA, LETI, F-38000 Grenoble, France, ‡Univ. Grenoble Alpes, CNRS, Grenoble INP, IMEP-LAHC, 3 Parvis Louis Neel, F-38000 Grenoble, France*

Ni-based contacts are envisioned for the integration of III-V / Si hybrid lasers on a 300 mm platform. In this paper, we present and compare the impact of in-situ preclean (PC) based on Argon (Ar) or Helium (He) plasmas over the resulting surface morphology, element distribution and phase formation sequence of the Ni / InP system. To do so, we combine several morphological and structural characterizations. Results point to the conclusion that Ar PC damages InP surfaces, while He PC does not. Ni deposition affects InP surfaces as well, by smoothing the differences between Ar and He precleaned surfaces. We con-clude that Ni deposition conditions are responsible for identical phase sequence on either Ar and He precleaned surfaces.

14:45 - 15:10
7.4. Contact Resistance Reduction for 7 nm FinFET Node and Beyond
Su-Chen Fan, Zuoguang Liu, Shogo Mochizuki, Juntao Li, Chris Waskiewicz, Adra Carr, Hemanth Jagannathan, Veeraraghavan S Basker, Teresa Wu, Brent Anderson, Dechao Guo, Huiming Bu
IBM Semiconductor Technology Research, 257 Fuller Road, Albany, NY 12203

We investigated contact resistance reduction with different techniques to increase active dopant density at contact and source / drain interface. A model is used to estimate the active dopant density increment vs contact resistance reduction. With epitaxy through contact and solid phase epitaxy techniques, about 60% contact resistance reduction is achieved with resistivity of 2x10-9 ohm-cm2.

15:10 - 15:30
PM break

Session 8 - Advanced Packaging
Royal A and B rooms, 1st floor
Session Chairs: Andrew Yeoh, *Intel*, Takahisa Furuhashi, *Sony*

15:30 - 16:00
8.1. INVITED - Integration and packaging technologies for combined microelectronic and photonic assemblies
Klaus Dieter Lang, *Fraunhofer*

Monolithic chip-level integration of electronics and photonics advances and increase I/O challenges in terms of photonic integration and packaging dramatically. Precise assembly capabilities and approaches are fundamentally demanded to provide reliable electronic interconnects and high optical coupling efficiency. Photonic interposers are promising integration platforms for photonics integrated circuits. The talk presents the key considerations in photonic and microelectronic integration and packaging, such as 3D integration, high precision assembly, thermal management, efficient optical coupling. Further, glass and silicon based photonic interposer technologies and respective applications discussed in detail. On board level thermal ion exchange as an example will be presented for graded index buried single mode optical waveguides in thin glass sheets which can be laminated within organic PCB stack-ups resulting in reliable electrical-optical circuit board interposer.

16:00 - 16:25
8.2. TSVFET - Vertical 3D Field-Effect Transistor
Felix Winkler1,2, Sebastian Killge1, Milan Pešić3 and Johann W. Bartha1,2
1Technische Universität Dresden, Institute of Semiconductors and Microsystems, IHM Dresden, Germany, 2Technische Universität Dresden, Center for Advancing Electronics Dresden, 01062 Dresden, Germany, 3MDLSoft inc, 5201 Great America Parkway, Santa Clara, CA, USA

A vertical Ru metal gate field-effect transistor (FET) has been manufactured in a through silicon VIA (TSV). Source and drain were defined by n-doping of the front side and back side of a 200 µm thin p-doped silicon wafer. The gate dielectric material was a stack of SiO2 and Al2O3. A saturation current of 10 µA for 4 V gate voltage and an on/off current ratio of > 10e6 could be shown.

16:25 - 16:50
8.3. Enhanced Reliability of Fan-Out Panel Level Package (FO-PLP) through Electromigration Evaluation of Redistribution Layer and Solder Joints
*Hyunjun Choi, Yoonkyeong Jo, Myung Soo Yeo, Jaewon Chang , Tae-Young Jeong, Jin-Hong Park, Eunmi Kwon, Youngseok Jung, Wooyeon Kim, Jinseok Kim, Junekyun Park, Hwasung Rhee and Sang-woo Pae
Foundry Division, Samsung Electronics, 1 Samsung-ro, Giheung-gu, Yongin-si, Gyeonggi-do 17113, Republic of Korea
Department of Semiconductor and Display Engineering, Sungkyunkwan University Suwon 16419, Republic of Korea

The fan-out technology can provide many advantages over the surface mount based packages, but the increase of current density in the redistribution layer (RDL) poses potential reliability risk. In order to evaluate the electromigration (EM) performance of the fan-out panel level package (FO-PLP), a series of EM tests have been conducted on the Sn-based solder ball and the RDL. First, the RDL EM test results showed that the time to fail (TTF) distribution was very tight, yielding a sufficient EM lifetime margin in the use condition. The root mean square (RMS) and peak current as well as the average current were quantified and fully verified from the experimental data. Also, the average EM and current sweep test were carried out on a 45° degree bended line to study the current crowding effect. From the experimental results, the bended shape wasn't a major factor affecting the average EM and peak current. In the solder joint EM results, it was found that the EM performance of the Ni under bump metallization (UBM) inserted solder joint was improved by 86% on the allowable maximum current basis. A Ni layer effectively has a role of diffusion barrier to Cu UBM consumption, suppressing EM induced void nucleation.

16:50 - 17:15
8.4. Electromigration Behavior of 2 um Pitch Cu/SiCN Hybrid Bonds
Joke De Messemaeker, Soon-Wook Kim, Michele Stucchi, Gerald Beyer, Eric Beyne and Kristof Croes
3D and Silicon Photonics Technologies imec Leuven, Belgium

Cu/SiCN to Cu/SiCN hybrid bonds with 360 nm top pads and 1080 nm bottom pads were tested in electro-migration (EM) with electrons flowing down. At these pad dimensions, failure is observed to occur only in the pads, without damage to the current feed lines. We propose that this failure is due to migration of the pre-existing voids at the bonding interface, along the surface of the bottom pad and the sidewall of the top pad, towards the top of the top pad, driven by the electric current. Therefore in sub 2 µm pitch hybrid pad-to-pad connections, void control at the bonding interface is key to EM performance. For interconnects with a large pad size difference, EM lifetime is predicted to be significantly enhanced when electrons are sent up towards the small pad.

17:15 - 17:40
8.5. Stress Evolution and Reliability Analysis in Integrated Fan-Out and Flip-chip Packages
*Xiaopeng Xu, *Simeon Simeonov, *Karim El-Sayed, Aditya P. Karmarkar
**Synopsys, Inc., Mountain View, CA, USA, Synopsys (India) Private Limited, Hyderabad, India*

Residual stresses and reliability are assessed in integrated fan-out (InFO) and conventional flip-chip (FC) packages using sequential package assembly simulation and various material models. The results indicate that InFO packages can have lower residual stresses and higher reliability as compared to FC packaging. It is observed that constituent materials must be selected carefully to improve reliability. Additionally, appropriate material models must be employed to accurately assess the structural reliability and failure probability for InFO and conventional FC packages

TECHNICAL PROGRAM: THURSDAY 6TH JUNE

Session 9 - Contacts 2

Royal A and B rooms, 1st floor
Session Chairs: Paul Besser, *ARM*, Dries Dictus, *Lam Research*

08:15 - 08:45
9.1. INVITED - Contact material and process for MOL
Junichi Koike, *Tohoku University*

This paper reports possible new materials to obtain low-resistivity local interconnections and possible ways to obtain low-resistivity contact aimed for 3 nm technology node.

08:45 - 09:15
9.2. INVITED - The ultra low emittance synchrotron storage ring ESRF-EBS: new opportunities for material characterization
Jean Susini, *ESRF*

The European Synchrotron Radiation Facility is Europe's premier hard X-ray synchrotron radiation source serving 45 experimental stations for public use. In 2009, the facility launched an ambitious upgrade programme covering all aspects of the facility, including photon production, experimental facilities for users, user service, and X-ray technology development. The upgrade benefits all areas of X-ray applications, such as imaging, spectroscopy and diffraction.

The Phase II of this upgrade programme (2015-2022) is focusing primarily on the design and construction of a new storage ring with the goal to reduce the horizontal emittance of the electron beam by a factor of 40 [1]. This project called Extremely Brilliant Source - ESRF-EBS - will lead to a dramatic increase in brilliance and coherence and will enable new applications for the study of soft and hard condensed matter, using X-rays. After an introduction of the main concepts behind this new revolutionary X-ray source, the new characterisation techniques and their potential for new applications will be discussed.

09:15 - 09:40
9.3. Annealing Ambient Effect on the EWF of CVD Molybdenum Deposited on a Tungsten Based Liner
*Ekaterina Zoubenko, *Moshe Eizenberg, Ilanit Fisher, Shruti Thombare, Patrick Van-Cleemput and Michal Danek
**Department of Materials Science and Engineering Technion – Israel Institute of Technology Haifa, Israel , CVD/ALD Advanced Metals C&F Lam Research Corporation Fremont, California*

This work is a thorough investigation of the structural and electrical stability of a MOS stack consisting of Molybdenum chemical vapor deposited on Tungsten carbo-nitride liner (different thicknesses) deposited on SiO2 by thermal atomic layer deposition. The purpose is to explore metallization schemes for future 3D logic and memory devices. An effective work function value of 4.8eV was determined for an as-deposited and for a vacuum annealed metal stack, while forming gas annealing led to a reduction of 0.2eV.

09:40 - 10:05
9.4. A New Cobalt Contact Structure Using Amorphous Si-Rich W Silicide Films
Naoya Okada, Noriyuki Uchida, Shinichi Ogawa, and Toshihiko Kanayama
National Institute of Advanced Industrial Science and Technology (AIST) Tsukuba, Japan

Cobalt is now recognized as the most possible metal alternative to W and Cu in contact and interconnect for advanced CMOS. Here we demonstrate that the electron Schottky barrier height (SBH) was reduced to 0.43 eV at Co/n-Si junctions by inserting an amorphous WSin (n = 8) film composed of W-atom-encapsulated Sin cage clusters, owing to the low work function close to the conduction band edge of Si. The SBH reduction effect was kept even after annealing up to at 500 °C.

The thermal stability was also confirmed by electrical resistivity measurements of the double layers of Co/WSin. Thus, the WSin film is a promising contact material at S/D with Co.

10:05 - 10:25
AM break

Session 10 - Quantum Computing and Modelling

Royal A and B rooms, 1st floor
Session Chairs: Tetsu Tanaka, *Tohoku University*, Mansour Moinpour, *Merck*

10:25 - 10:55
10.1. INVITED - Challenges for Quantum Processors Based on Superconducting Circuits
Martin Sandberg, *IBM*

Superconducting quantum circuits have emerged as a prime contender for implementing quantum processors, with the goal of realizing universal quantum computing. Due to the significant hardware overhead required for error-correction, fault-tolerant quantum computation is still some time away in the future, but smaller, noisy intermediate-scale quantum (NISQ) processors are already available today, such as the IBM Q Experience (www.research.ibm.com/ibm-q).
Scaling superconducting quantum circuits further requires new experimental advances and hardware developments. In addition to increasing the number of quantum bits (qubits) on a chip, larger quantum circuits require qubits with longer coherence times, better hardware integration, and improved system level performance, including improvements at the packaging level. To assess the power of a quantum processor in the near term, we propose a metric called the quantum volume, which is agnostic to the particular implementation and architecture of a quantum computer.

10:55 - 11:20
10.2. Fabrication of Superconducting Resonators in a 300 mm Pilot Line for Quantum Technologies
Danny Wan1, Johan Swerts1, Laurent Souriau1, Jonathan Burnett2, Xiaoyu Piao1, Massimo Mongillo1, Jeroen Verjauw1, Anton Potocnik1, Arame Thiam1, Julien Jussot1, Diziana Vangoidsenhoven1, Antoine Pacco1, Marina Kudra2, David Niepce2, Tsvetan Ivanov1, Guillaume Boccardi1, Dan Mocuta1, Jonas Bylander2, and Iuliana Radu1
1 imec, Kapeldreef 75, B-3001 Leuven, Belgium, 2 Chalmers University of Technology, Microtechnology and Nanoscience, SE-412 96, Göteborg, Sweden

Superconducting microwave resonators of TiN, Nb, and NbN were fabricated in imec's 300 mm pilot line utilizing an advanced production toolset. Deposited materials were screened and thoroughly characterized before and after patterning. Resonator quality (Q) factor at single photon energies was observed to vary over several orders of magnitude ranging from 1k to 300k depending on the fabrication process. While, amorphous materials at critical interfaces were found to limit the measured Q factor, material and patterning development in a 300 mm environment can offer a path towards better control and reproducibility when fabricating superconducting resonators and other quantum circuits.

11:20 - 11:45
10.3. Copper Electromigration; Prediction of Scaling Limits
Houman Zahedmanesh, Olalla Varela Pedreira, Chris Wilson, Zsolt Tőkei, Kristof Croes
imec Leuven, Belgium

In this paper simulations are employed to predict the scaling limits of Cu interconnects due to electromigration. The simulations identified a continuously decaying trend of jmax with reduction of linewidth. Reducing the linewidth to 10 nm resulted in a drop of jmax to below 1 MA/cm2 even with Co cap. For the short length effect, the model highlights the importance of flux divergence point for scaled barrier thicknesses. It is predicted that only 5% material flux through the barrier at the anode end of a 10 nm wide short line (i.e. 5 μm length operating under j<jc at 100˚C), will drastically reduce the lifetime.

11:45 - 12:10
10.4. Process Modeling Exploration for 8 nm Half-Pitch Interconnects
A. Soussou, B. Vincent, J. Ervin*, 1B. Briggs, 1S. Decoster, 1C. J. Wilson,
*COVENTOR 3, Avenue du Québec, 91140 Villebon sur Yvette, France *135 Beaver Street, Waltham, Massachusetts, United States*
1IMEC Kapeldreef 75, 3001 Heverlee, Belgium

In this paper, we simulate eSADP, eSAQP and iSAOP patterning options to enable fabrication of 8 nm Half-Pitch (HP) interconnects. We investigate the impact of process variations and patterning sensitivities on pitch walking and resistance performance. The overall yield is also calculated for eight line CDs as well as M2-via-M1 via segment resistance and compared for all options. Process sensitivity simulation results enable us to evaluate the most robust options for 8 nm HP patterning.

12:10 - 13:25
Lunch

Session 11 - Beyond Copper 2

Royal A and B rooms, 1st floor
Session Chairs: Soo-Hyun Kim, *Yeungnam University*, Sylvain Maitrejean, *CEA-Leti*

13:25 - 13:55
11.1. INVITED - Approaches and challenges for self-aligned fabrication by area-selective atomic layer deposition
Adrie Mackus, *Eindhoven University of Technology*

The increasingly demanding requirements for alignment in semiconductor processing currently motivate the development of bottom-up and self-aligned fabrication schemes based on area-selective atomic layer deposition (ALD). For instance, area-selective ALD of dielectric-on-dielectric in the presence of metal areas is considered for the fabrication of reliable interconnects using a fully self-aligned via (FSAV) scheme. These applications require area-selective ALD processes for a broader range of materials and improvement of the selectivity that can be achieved.

A new strategy for area-selective ALD was recently developed involving the dosing of inhibitor molecules in ABC-type (i.e. three-step) cycles.[1] The use of small inhibitor molecules that can be dosed in vapor-phase makes this strategy compatible with industrial process flows. Furthermore, the reapplication of the inhibitor molecules during every cycle allows for employing plasma-assisted ALD, thereby enabling area-selective ALD for more material systems. Proof-of-concepts results will be presented for area-selective ALD of SiO2, and the underlying mechanisms of precursor blocking by inhibitor molecules will be discussed.

One of the main challenges in the field of area-selective ALD is to meet the requirements for selectivity in semiconductor processing.[2] Current research efforts focus on combining area-selective ALD with atomic layer etching (ALE) processes as the approach for improving the selectivity.[2],[3] This approach will demonstrated for area-selective ALD of Ru using an etching cycle of O2 plasma and H2 gas. New opportunities offered by these advanced ALD/ALE cycle schemes will be described.

13:55 - 14:20
11.2. Low Resistivity NiAl and CuAl2 Thin Films as Copper Alternatives
Linghan Chen, Daisuke Ando, Yuji Sutou and Junichi Koike
Department of Materials Science, Tohoku University, Sendai 980-8579, Japan

This paper reports NiAl and CuAl2 intermetallic compounds as new interconnect materials to replace Cu for advanced technology nodes. Adhesion strength, diffusion-barrier property and film resistivity were investigated for both compounds, and gap-filling capability was investigated for CuAl2. The obtained results indicated that both NiAl and CuAl2 could be used without liner and barrier layers for narrow line width/thickness below 10 nm.

14:20 - 14:45
11.3. Oxygen-free Atomic Layer Deposition of Ruthenium for BEOL Applications
Guo Liu, Jacob Woodruff, Dan Moser, Mansour Moinpour, Ravi Kanjolia
EMD Performance Materials Corp. Haverhill, Massachusetts, USA A Business of Merck KGaA, Darmstadt, Germany

ALD growth of ruthenium using (DMBD)Ru(CO)3 with a series of O2-free co-reactants has been investigated. Precursor properties were compared with other previously published Ru precursors. The oxygen-free co-reactant deposition is demonstrated at temperatures in the range of 200-250°C with high growth rate and short nucleation delays. A post deposition anneal of 400°C in an inert gas atmosphere was shown to reduce resistivity, matching that of more conventional O2 based Ru ALD processes. We also demonstrate that better quality Ru film by this oxygen-free ALD process can be deposited on a metal nitride liner to reduce grain size and improve film roughness and conformality.

14:45 - 15:10
11.4. Electromigration activation energies in ruthenium interconnects
S. Beyne1,2, O. Varela Pedreira2, H. Oprins2, I. De Wolf 1,2, Zs. Tőkei2 and K. Croes2
1MTM, KU Leuven, Kasteelpark Arenberg 44 bus 2450, B-3001, Leuven, Belgium, 2imec, Kapeldreef 75, B-3001, Leuven, Belgium

The activation energy (EA) of Ru interconnects is determined by low-frequency noise (LFN) measurements. Values of ~1eV are found. Wafer level accelerated electromigration (EM) tests were carried out to compare the LFN EA to the EM EA. The calculation of the EM EA is found to be strongly dependent on the temperature profile in the wire due to Joule heating (JH). The temperature profile was calculated analytically, assuming the contacts are at ambient temperature. For a void forming in direct proximity of the contact, the EM EA matches the LFN EA. For a void at average wire temperature (ambient + JH), EA ~ 2eV. In addition to demonstrating the application of LFN to study EM in alternative metals, this paper also cautions for the impact of JH on the calculation of EA in interconnects.

15:10 - 15:30
PM Break

Session 12 - Reliability
Royal A and B rooms, 1st floor
Session Chairs: Kazuyoshi Ueno, *Shibaura Inst Tech.*, Christian Witt, *Global Foundries*

15:30 - 16:00
12.1. INVITED - Overview and challenges in the metallization of 3D NAND devices
Inhee Lee, Chaio Chung, Euiseong Hwang, Sunggon Jin, Seungho Pyi, *R&D Process Center, SK Hynix, Icheon, South Korea*

3D NAND product using 24 layers and MLC has successfully been in the market since August 2013 with expectation that it will rapidly reduce the cost of NAND and replace planar NAND. Though chip makers of 3D NAND have all announced production plans for 3D NAND with 96 layers using TLC in five years later, 2018, 3D NAND is still more expensive than planar NAND and has several technical issues. Therefore, I would like to discuss what the 3D NAND's process challenges are, and what might be its ceiling, as increasing numbers of layers are used.

16:00 - 16:25
12.2. Scaled TaN barriers for Cu interconnects: Reliability performance
O. Varela Pedreira, A. Leśniewska, N. Jourdan, V. Vega Gonzalez, S. Lariviere, M.H. van der Veen, K. Croes, Zs. Tőkei
imec Leuven, Belgium

One approach to continue the use of Cu in advanced nodes is to reduce the thickness of the barrier and liner. This reduction will allow more Cu in the trench that will reduce the global resistance of the wires and vias. We study the reliability performance of scaled PVD TaN barriers with a CVD Co or Ru

liner in integrated structures. TDDB measurements show that all studied systems keep their Cu barrier properties when measured at 100°C. CCS-TVS measurements show Cu gets mobile at 200°C suggesting defects are present in our barrier/liner systems, where their impact on reliability at lower temperatures remain unclear. Regarding electromigration, we see a difference between using Co or Ru liner. While for a 3nm TaN/1nm Co system we observed voids in some vias, for scaled TaN barriers in combination with Ru liners, we only observed voids along the line suggesting the TaN/Ru barrier liner system is more scalable. An average EA of about 0.9eV was observed for all the TaN/Ru systems, as expected for a system with SiCN cap. This results confirm that TaN/Ru is more scalable towards smaller dimensions making it a promising candidate in advanced nodes.

16:25 - 16:50
12.3. EM enhancement of Cu interconnects with Ru liner for 7 nm node and beyond
K. Motoyama1, O. van der Straten1, J. Maniscalco1, K. Cheng1, S. DeVries1, C.-K. Hu1, H. Huang1, K. Park2, Y. Kim2, S. Hosadurga1, N. Lanzillo1, A. Simon1, L. Jiang1, B. Peethala1, T. Standaert1, T. Wu1, T. Spooner1, and K. Choi1
1IBM Research, 2Samsung Electronics Co. LTD., Albany Nanotech, 257 Fuller Rd., Albany, NY 12203

Highly reliable Cu interconnects with CVD Ru liner have been demonstrated for the 7 nm node. It has been observed that void-free Cu fill, interface control for both Cu/liner (trench sidewall and bottom) and Cu/cap (trench top), and grain size engineering are critical to improve Electromigration (EM) performance for Cu interconnects with Ru liner. This study focused on optimizing the metal barrier process, post Ru liner deposition treatment, the Cu fill process, and Ru CMP process.

16:50 - 17:15
12.4. Joule Heating study in scaled Cu, Co and Ru interconnects
Melina Lofrano, Olalla Varela Pedreira, Kristof Croes and Zsolt Tőkei
imec Leuven, Belgium

We discuss Joule heating effects in scaled interconnects, where Ru and Co lines have been compared with standard Cu interconnects. Due to the combination of a high electrical resistivity of the metal and a poor thermal conductivity of the IMD, the Joule heating in these lines is significantly higher compared to Cu lines. Using a finite element model that is calibrated at wider dimensions (22nm lines width), we predict that Joule heating in 10nm wide lines can become significant at use conditions. We also shown that the IMD plays an important role on the Joule heating effect, where we show that integrating metal lines in an IMD with a higher thermal conductivity leads to a significantly reduced Joule heating and consequently its effect on the neighboring lines can be limited as well.

17:15 - 17:30
End of conference